Accelerate Your Time-to-Mission™

Discrete I/O EF
DT5
Function Module

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	2/1/2018	Initial release	SL
A1	2/13/2018	ECO C05364, update to title page	SL
A2	3/5/2018	ECO C05412, updates to module manual consistency	SL
A3	8/15/2018	ECO C05798, correction to Pattern Ram Control register	SL

Table of Contents

Introduction

This module manual provides information about the North Atlantic Industries, Inc. (NAI) Discrete Function Module: DT5. This module is compatible with all NAI Generation 5 motherboards.

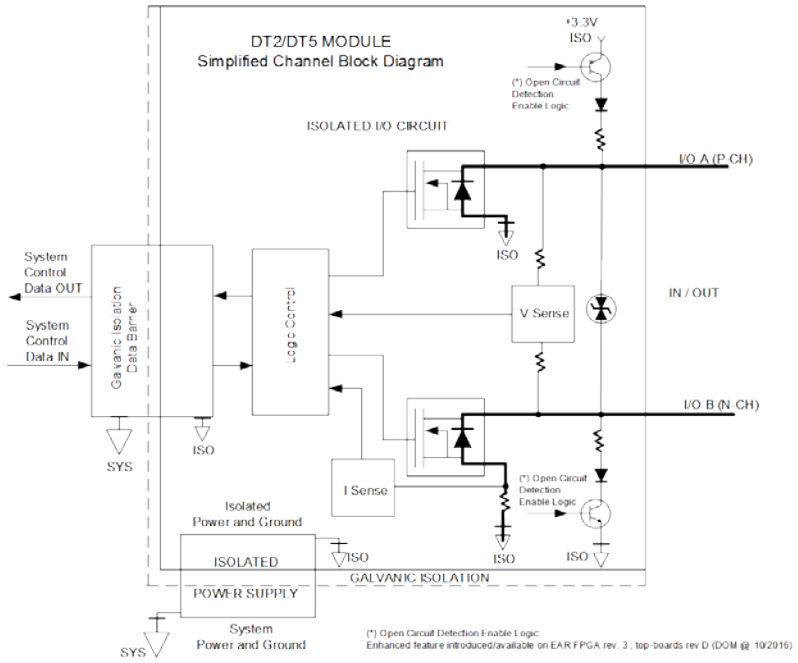
The DT5 Discrete module is a digital I/O 32-Bit Enhanced Functionality module that provides 16 individual channels that either can be used for input voltage measurements, or as a bidirectional current switch. The channels are programmable in enhanced mode to enable Pulse Width Modulation, Pattern Generation and Pulse Timing measurement capability.

Features

- 16 channels available as inputs or outputs
- Programmable for Input voltage or switch closure for each channel
- Continuous background built-in-test (BIT) (during normal operation, status provided for channel health and operation feedback)
- In bidirectional current switch mode, enhanced features can be used to trigger switch opening or closure using pulse width, number of pulses or pattern generation
- Ability to read switch I/O voltage and current
- Ability to handle switch closure currents of up to 625 mA DC
- Automatic switch overcurrent protection, programmable to 625 mA max
- Open Circuit Detection
- Supports ‘dual turn-on’ (series channel output) applications (e.g. dual series ‘key’ missile launch control)
- Clean, bounce-free switching

Specifications

Discrete I/O - 16-Channel EF Module DT5



INPUT CHARACTERISTICS

Input Range:	±80 V (peak) / ±60 V (typical)
Input Pulse Detection:	A pulse of 40µs min. width will be sensed and indicated by the appropriate Hi–Lo or Low-High Transition Interrupt.
Input Impedance:	2 MΩ / (200 kΩ if/when Open Circuit Detect Logic enabled)
Switching Threshold:	Levels are programmable from 0 to 80 Vrms with 10-bit resolution (0.98% FS) On/Off.
Accuracy of Set Point:	The greater of 5% signal value or 0.25 V.
ON/OFF Differential	0.5 V min. recommended.
Debounce:	Programmable per channel from 0 to 10µs x 2^{32} (LSB= 10 µs; 32-bit resolution).
Update Rate:	Each channel is updated every 10 µs.
Overvoltage Protection:	Input clamped at ±80 VDC.
Voltage Measurement:	User can read output voltage of each channel (isolated 10-bit A/D) LSB=100mV; Accuracy: ±3 LSB's (300 mV) over temperature.
Additional Enhanced Input Mode Operation:	Input with debounce filter (Mode 0), measure High Time (Mode 1), measure Low Time (Mode 2), time-stamp of all rising edges (Mode 3), time-stamp of all falling edges (Mode 4), time-stamp of all edges (Mode 5), count total number of rising (Mode 6), falling (Mode 7), all (Mode 8) edges, measure period from rising edge-to-rising edge (Mode 9), measure frequency (Mode 10).

BIDIRECTIONAL SWITCH

Switch Formats:	Isolated bidirectional (AC/DC) MOSFET switch
Switch Current:	0-625 mA per channel (load determined) / (±80 V peak)
Switch Impedance Open:	2 MΩ / (200 kΩ if/when Open Circuit Detect Logic enabled)
Switch Impedance Closed:	0.5 W typical, 1 W max.
Current Measurement:	User can read AC/DC current through switch, independently for each channel, LSB=3 mA; Accuracy: The greater of ±10% of Signal or ±20mA over temperature.
Measurement Update Rate:	Each channel is updated every 10 µs.
Isolation:	500 V (between channels and each channel to system GND).
Power:	5 VDC/0.98 A max.
Weight:	1.5 oz. (42 g)
Additional Enhanced Output Mode Operation:	PWM Continuous Output, PWM Burst (n-times), and Pattern Generator Output.

Specifications are subject to change without notice.

Principle of Operation

DT5 provides 16 independent, isolated, programmable channels that either can be used for input voltage measurements (+/-60 V), or as a bidirectional current switch (up to 625 mA per channel). With the switch closed, both the current through the switch and the voltage across the switch can be monitored. These modules include diode clamping on each channel. Clamping is useful for inductive loads, such as relays and short circuit protection.

The DT5 Mode Select register provides 13 Mode settings. Each channel can be set to any of the different input or output modes. All settings provide BIT fault detection, which enables flagging of non-compliant outputs or inconsistent input readings between dual input measurements.

All 16 channels are galvanically isolated from each other and from system ground. Each channel's two-wire connection can function as an isolated voltage input or as an isolated bidirectional switch. When programmed to function as a bidirectional switch, a channel can control valves mechanical relays, indicators, etc. without concern about grounding. This module provides an automatic background built-in-test (BIT) for each channel. The BIT functions are always enabled and continually check that each channel is functioning properly.

Standard input operation is used for voltage sensing and measures both AC and DC input voltages. When operating as a switch, measurements for both voltage across and current through the switch closure are available. Current and Voltage measurements are available as both instantaneous and averaged (RMS).

Four input voltage threshold levels (Maximum High, Upper, Lower, Minimum Low) are programmed to user defined high and low voltage levels. All four of the threshold levels must be set for each Input or Output channel. Threshold crossing may be programmed to generated interrupts on a change of state.

The module design utilizes state of the art galvanic isolation that is superior to alternatives such as optocoupler devices. The galvanic isolation eliminates typical optocoupler design concerns such as uncertain current transfer ratios, nonlinear transfer functions and temperature/lifetime degradation effects.

Input/Switch Interface

Each channel contains a both an isolated differential amplifier and a dual N-Channel MOSFET, configured as isolated Solid-State Relay (SSR). The SSR is energized, so both AC and DC current can flow through the channels I/O pins. The MOSFET presents a low ~.5 Ω on impedance. The module contains circuitry to measure the current through the SSR and the voltage present on the I/O pins.

Open Circuit Detection

Each of the 16 channels can be set to indicate an open circuit by setting the *Open Circuit Detection* register for the channel to 1. A voltage reading of 3.3 V indicates that the channel is open. Default (normal operation) is 0 V. Set the *Maximum High Threshold* register, for each channel, to this value to generate an interrupt using the *Maximum High Threshold Interrupt Enable* register.

Note: Added Enhanced Feature; introduced/available on EAR FPGA rev. 3; top-boards rev D (DOM @ 10/2016).

Register Descriptions

The register descriptions provide the register name, Register Offset, Type, Data Range, Read or Write information, Initialized Value, a description of the function and, in most cases, a data table.

Read I/O

Function: Reads High **1** or Low **0** inputs or outputs as defined by internal channel threshold values.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: NA

Operational Settings: NA

Read I/O																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Switch Control

Function: Opens and closes the switch for each channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0x 0000 0000

Operational Settings: Write **0** for input; Write **1**, for closed switch.

Switch Control																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Open Circuit Detection

Function: Enables a 3.3v pull-up on the channel that may be used for open circuit detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0x0000 0000

Operational Settings: Write integer **1** for open circuit detection. Default is **0**, which does not provide open circuit detection. When an open circuit occurs, the voltage read on the channel will be pulled up to ~2.7 V. Normal reading is 0.

An interrupt is generated for open circuit indication, by channel, via the *Maximum High Threshold* and *Maximum High Threshold Interrupt Enable* registers.

Note: Added Enhanced Feature; introduced/available on EAR FPGA rev. 3; top-boards rev D (DOM @ 10/2016).

Open Circuit Detection																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Switch State

Function: Reads whether the state of the switch is open or closed.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: N/A

Operational Settings: N/A

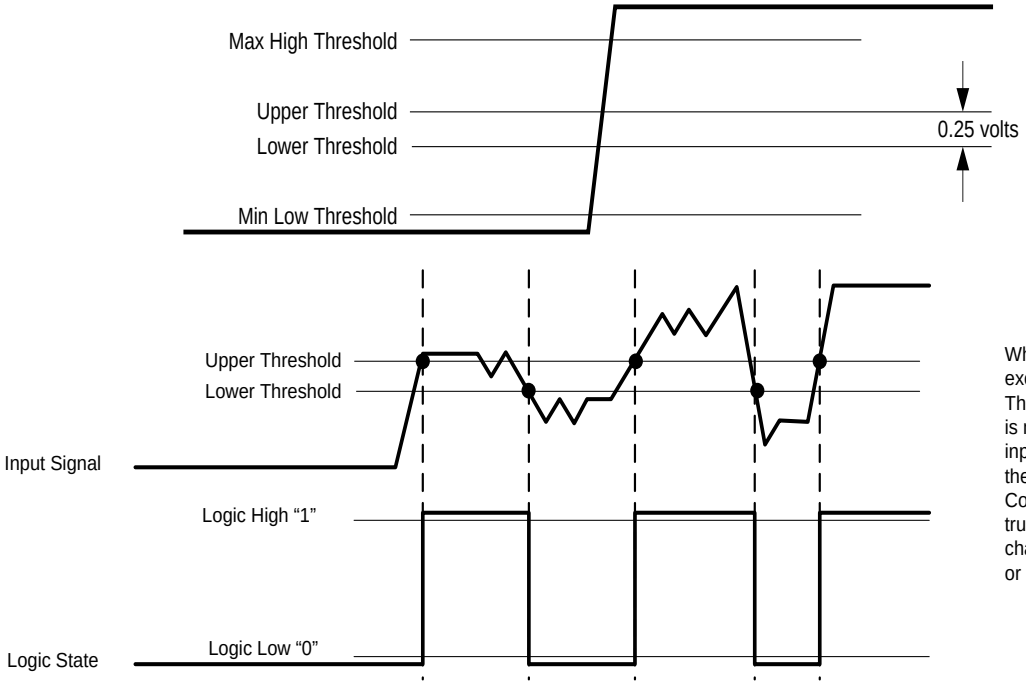
Switch State																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Threshold Programming

Four threshold levels: Maximum High, Upper, Lower, Minimum Low offer maximum user flexibility. All four threshold levels must be programmed. For input or output, the threshold levels will define the logic states. For proper operation, the threshold values should be programmed such that:

Maximum High Threshold > Upper Threshold > Lower Threshold > Minimum Low Threshold

Program Upper and Lower Thresholds, keeping the 0.25 V min. differential in mind, and then add debounce time as required. When the input signal exceeds the Upper Threshold, a logic high **1** is maintained until the input signal falls below the Lower Threshold. Conversely, when the input signal falls below the Lower Threshold, a logic low **0** is maintained until the input signal rises above the Upper Threshold.



When the input signal exceeds the Upper Threshold, a logic high "1" is maintained until the input signal falls below the Lower Threshold. Conversely, the same is true as the signal changes from low to high, or high to low.

Maximum High Threshold

Function: Sets the maximum high threshold value. Programmable per channel from -60 to +60 Vrms, with binary 10-bit word resolution (LSB=100 mv).

Type: binary word (32-bit)

Data Range: 0x FFFF FDA8 to 0x 0000 0258 (usable range)

Read/Write: R/W

Initialized Value: 0x64

Operational Settings: Assumes that the programmed level is the minimum voltage used to indicate a Max. High Threshold. If a signal is greater than the Maximum High Threshold value, a flag is set in the *Maximum High Threshold* register. The *Maximum High Threshold* register may be used to monitor any type of high signal voltage condition or threshold such as a "Short to +V" as it applies to input measurement as well as contact sensing applications.

Maximum High Threshold																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Upper Threshold

Function: Sets the upper threshold value. Programmable per channel from -60 to +60 Vrms, with binary 10-bit word resolution (LSB=100 mv).

Type: binary word (32-bit)

Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)

Read/Write: R/W

Initialized Value: 0x32

Operational Settings: A signal is considered logic High (**1**) when its value exceeds the Upper threshold and does not consequently fall below the Lower threshold in less than the programmed Debounce time.

Upper Threshold																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lower Threshold

Function: Sets the lower threshold value. Programmable per channel from -60 to +60 Vrms, with binary 10-bit word resolution (LSB=100 mv).

Type: binary word (32-bit)

Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)

Read/Write: R/W

Initialized Value: 0x1E

Operational Settings: A signal is considered logic Low (**0**) when its value falls below the Lower threshold and does not consequently rise above the Upper Threshold in less than the programmed Debounce time.

Lower Threshold																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Minimum Low Threshold

Function: Sets the minimum low threshold. Programmable per channel from -60 to +60 Vrms, with binary 10-bit word resolution (LSB=100 mv).

Type: binary word (32-bit)

Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: Assumes that the programmed level is the maximum voltage used to indicate a minimum low threshold. If a signal is less than the Minimum Low Threshold value, a flag is set in the *Minimum Low Threshold Status* register. The *Minimum Low Threshold* register may be used to monitor any type of low signal voltage condition or threshold such as a “Short to Ground” as it applies to input measurement as well as contact sensing applications.

Minimum Low Threshold																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Debounce Time

Function: Sets the Debounce time (LSB= 10 µs; 32-bit resolution) for each channel.

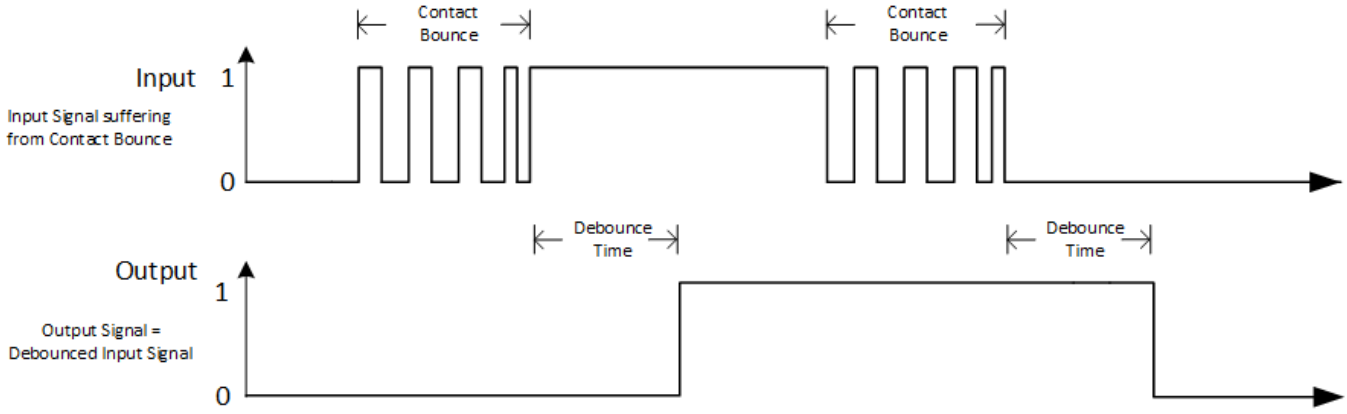
Type: binary word (32-bit)

Data Range: 0x 0000 0000 to 0x FFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: The Debounce register, when programmed for a non-zero value, is used with channels programmed as input to “filter” or “ignore” expected application spurious initial transitions. Enter required debounce time into appropriate channel registers. LSB weight is 10 µs/bit (register may be programmed from 0x00000000 (debounce filter inactive) through a maximum of 0xFFFFFFFF (2^32 * 10µs). (full scale w/ 10 µs resolution). Once a signal level is a logic voltage level period longer than the debounce time (Logic High and Logic Low), a logic transition is validated. Signal pulse widths less than programmed debounce time are filtered. Once valid, the transition status register flag is set for the channel and the output logic changes state. Enter a value of 0 to disable debounce filtering. Debounce defaults to 0000h upon reset.



Voltage Reading (Sampled)

Function: Reads actual output voltage at I/O pin per individual channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)
Read/Write: R
Initialized Value: Updated by module as per conditions
Operational Settings: Value is a signed binary 32-bit word, where LSB = 100 mV. Data is read as 2's complement number. For example, if output voltage word is 0x00F0 (240d), actual voltage is 24.0 V.

Voltage Reading (Sampled)																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Voltage Reading (Averaged)

Function: Reads averaged RMS value of the output voltage at I/O pin per individual channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)
Read/Write: R
Initialized Value: Updated by module as per conditions
Operational Settings: Value is an unsigned binary 10-bit word, where LSB=100 mV. For example, if output voltage word is 0x00F0 (240d), actual voltage is 24 V.

Voltage Reading (Averaged)																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Current Reading (Sampled)

Function: Reads actual current through the I/O pins at each channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FEC8 to 0x0000 0138
Read/Write: R
Initialized Value: Updated by module as per conditions
Operational Settings: Value is signed binary 32-bit word, where LSB=2 mA. Read as 2's complement; Current source is positive, Current sink is negative. For example, if output voltage word is 0x 0064 (100d), actual current is 200 mA.

Current Reading (Sampled)																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Current Reading (Averaged)

Function: Reads averaged RMS current through the I/O pins at each channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FEC8 to 0x0000 0138
Read/Write: R
Initialized Value: Updated by module as per conditions
Operational Settings: Value is signed binary 32-bit word, where LSB=2 mA. Read as 2's complement; Current source is positive, Current sink is negative. For example, if output voltage word is 0x0064 (100d), actual current is (current source) 200 mA.

Current Reading (Averaged)																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Overcurrent Value

Function: Sets the current value at which the channel will detect an overcurrent condition.

Type: binary word (32-bit)

Data Range: 0x0000 0000 to 0x0000 0138

Read/Write: R/W

Operational Settings: LSB = 2 mA

Status and Interrupt Registers

The registers may be set for any or all channels and will latch if a transition is detected on a channel or channels. Each channel(s) will remain latched until the channel is cleared. Multiple channels may be cleared simultaneously, if desired. Each channel bit in the register is polled for a read status. Any subsequent channel(s) transition, if detected, will propagate through to be read (rolling-latch).

Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel) location (bit mapped per channel), will "clear" the bit (set the bit to **0**) if the actual interruptible event condition has cleared. If the interruptible condition "event" is still persistent while clearing, this may retrigger the interrupt.

There is a corresponding Interrupt Enable and vector associated with each "Latched" Status. Each status type may be "polled" (at any time), or is "interruptible" when interrupts are enabled and the associated Interrupt Service Routine (ISR) vectors are programmed accordingly. When programmed for "interruptible" status, interrupts are typically generated and flagged with the programmed vector available as data. The host or single board computer (SBC) typically services the interrupt by a general or specific ISR, which reads the (typically) unique programmed vector (identifier of which status generated the interrupt), reads the associated status register to determine which channel in the status register was "flagged" and then "clears" the status register. This essentially resets the interrupt mechanism, which is now ready to be triggered by the next status register detected event "flag". "Latched Status" will trigger on either "sense on edge" or "sense on level" based on the settings of the associated Set Edge/Level Interrupt register. Sense on "edge" requires a change from low to high state to trigger the status detection, while sense on "level" is independent of the previous state. Unless otherwise specified, all status or fault indications are bit set per channel.

BIT Dynamic Status

Function: BIT Dynamic Status is set when a redundant measurement is inconsistent with the input measurement level detected.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: 1 is read when a fault is detected. **0** indicates no fault detected.

BIT Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

BIT Latched Status

Function: The *BIT Latched Status* register is set when a redundant measurement is inconsistent with the input measurement level detected.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: **1** is written when a fault is detected. **0** indicates no fault detected. Write a **1** to clear status.

Notes: Faults are detected (associated channel(s) bit set to **1**) within 10 ms (pending characterization).

BIT Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

BIT Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *BIT Latched Status* register indicates a fault.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

BIT Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

BIT Set Edge/Level Interrupt

Function: Sets *BIT Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

BIT Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Dynamic Status

Function: Senses an overcurrent or overload condition for each channel and provides real-time status. The output channel is also immediately disabled at time of overcurrent sensed condition.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: 1 is read when overcurrent or overload condition transition is sensed. **0** indicates normal status.

Notes: Status is indicated (associated channel(s) bit set to **1**), within 80 ms (pending characterization).

Overcurrent Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Latched Status

Function: The *Overcurrent Latched Status* register is set when the channel senses an overcurrent or overload condition and provides latched status. The output channel is also immediately disabled at time of overcurrent sensed condition.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: 1 is written when overcurrent or overload condition transition is sensed. **0** indicates no status. Write a **1** to clear status.

Notes:

- Channel(s) shut down by overcurrent sensed can be reset by writing to the *Overcurrent Reset* register.

Overcurrent Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *Overcurrent Latched Status* register senses an overcurrent or overload condition for any channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Overcurrent Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Set Edge/Level Interrupt

Function: Sets *Overcurrent Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Overcurrent Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Reset

Function: Resets disabled channels in *Overcurrent Latched Status* register following an overcurrent condition as measured by the *Current Reading (Sampled) Register* and the value set by the *Overcurrent Value* register.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: 1 is written to reset disabled channels. Processor will write a **0** back to the *Overcurrent Reset* register when reset process is complete.

Overcurrent Reset																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	24	23	22	21	20	19	18	17	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Max Hi Threshold Dynamic Status

Function: Indicates voltage signal has exceeded Maximum High Voltage level. Real-time event status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: Dynamic Status is set when the voltage is above the Max Hi Threshold set in the *Maximum High Threshold* register. The associated channel(s) bit is set to **1** and is non-latching.

Max Hi Threshold Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Max Hi Threshold Latched Status

Function: The *Max Hi Threshold Latched Status* register is set when the voltage signal has exceeded Maximum High Voltage level set in the *Maximum High Threshold* register.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Status is indicated (bit is set) within 500 µs (pending characterization). Write a **1** to clear status.

Max Hi Threshold Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Max Hi Threshold Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *Max Hi Threshold Latched Status* register senses that the voltage signal has exceeded Maximum High Voltage level.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Maximum High Threshold Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Max Hi Threshold Set Edge/Level Interrupt

Function: Sets *Max Hi Threshold Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Maximum High Threshold Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Min Lo Threshold Dynamic Status

Function: Indicates voltage signal has fallen below Minimum Low Voltage level. Real-time event status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: Dynamic Status is set when the voltage is below the value set in the *Minimum Low Threshold* register. The associated channel(s) bit is set to **1** and is non-latching.

Min Lo Threshold Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Min Lo Threshold Latched Status

Function: The *Min Lo Threshold Latched Status* register is set when the voltage signal has fallen below Minimum Low Voltage level set in the *Minimum Low Threshold* register.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Status is indicated (bit is set) within 500 µs (pending characterization). Write a **1** to clear status.

Min Lo Threshold Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Min Lo Threshold Interrupt Enable

Function: When enabled interrupts are generated for each channel when the *Below Min Lo Threshold Latched Status* register senses the voltage signal has fallen below the Minimum Low Voltage level.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Min Lo Threshold Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Min Lo Threshold Set Edge/Level Interrupt

Function: Sets *Min Lo Threshold Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Min Lo Threshold Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Mid-Range Dynamic Status

Function: Indicates voltage signal is in-between Upper and Lower thresholds. Real-time event status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: Dynamic Status is set when the voltage is in between the values set in the *Upper Threshold* and *Lower Threshold* registers. The associated channel(s) bit is set to **1** and is non-latching.

Mid-Range Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Mid-Range Latched Status

Function: The *Mid-Range Latched Status* register is set when the voltage signal is in-between Upper and Lower thresholds set in the *Upper Threshold* and *Lower Threshold* registers.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Status is indicated (bit is set) within 500 µs (pending characterization). Write a **1** to clear status.

Mid-Range Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Mid-Range Interrupt Enable

Function: When enabled interrupts are generated for each channel when the *Mid-Range Latched Status* register senses the voltage signal is in-between Upper and Lower thresholds.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts

Mid-Range Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Mid-Range Set Edge/Level Interrupt

Function: Sets *Mid-Range Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Mid-Range Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	24	23	22	21	20	19	18	17	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lo-Hi Transition Dynamic Status

Function: Senses Low to High transitions for each channel and provides real-time status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: 1 is read when a rising edge transition is sensed. **0** indicates no status.

Notes: Considered “momentary” during the actual event when detected. Programmable for level or edge sensing, status is indicated (associated channel(s) bit set to **1**) within 20 µs (pending characterization).

Lo-Hi Transition Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lo-Hi Transition Latched Status

Function: The *Lo-Hi Transition Latched Status* register is set when it senses Low to High transitions for each channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: **1** is written when a rising edge transition is sensed. **0** indicates no status. Write a **1** to clear status.

Notes: Programmable for level or edge sensing, status is indicated (associated channel(s) bit set to **1**) within 20 µs (pending characterization).

Lo-Hi Transition Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lo-Hi Transition Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *Lo-Hi Transition Latched Status* register senses a Low to High transition for any channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Lo-Hi Transition Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lo-Hi Transition Set Edge/Level Interrupt

Function: Sets *Lo-Hi Transition Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Lo-Hi Transition Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Hi-Lo Transition Dynamic Status

Function: Senses High to Low transitions for each channel and provides real-time status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: 1 is read when a rising edge transition is sensed. **0** indicates no status.

Notes: Considered “momentary” during the actual event when detected. Programmable for level or edge sensing, status is indicated (associated channel(s) bit set to **1**) within 20 µs (pending characterization).

Hi-Lo Transition Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Hi-Lo Transition Latched Status

Function: The *Hi-Lo Transition Latched Status* register is set when it senses High to Low transitions for each channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: **1** is written when a falling edge transition is sensed. **0** indicates no status. Write a **1** to clear status.

Notes: Programmable for level or edge sensing, status is indicated (associated channel(s) bit set to **1**) within 20 µs (pending characterization).

Hi-Lo Transition Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Hi-Lo Transition Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *Hi-Lo Transition Latched Status* register senses a High to Low transition for any channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Hi-Lo Transition Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Hi-Lo Transition Set Edge/Level Interrupt

Function: Sets *Hi-Lo Transition Latched Status* register to trigger on edge or level detection.
Type: binary word (32-bit)
Read/Write: R/W
Initialized Value: 0
Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Hi-Lo Transition Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Enhanced Functionality

Input Modes

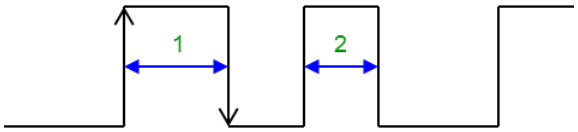
There are 10 Input modes. All input modes may be configured with debounce capability. Debounce capability allows configurable filtering of noisy signals and transients. Each channel may be set to an individual debounce time value. When a debounce time is set to a non-zero value, the signal reading after a transition must remain at the same level for the debounce interval before it is propagated through, otherwise it is rejected. All Input Modes (1-10) FIFO buffers are 1024 words deep.

Mode 0 – No Enhancement Mode

Behaves the same as a standard functionality only module.

Mode 1 – High Time Pulse Measurement (FIFO Buffer)

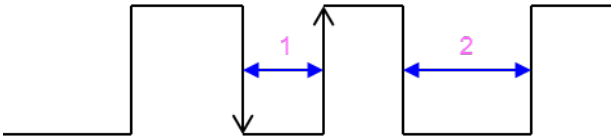
Timing measurements record the time interval (in 10 µs ticks) from a pair of transitions.



Pulse High, Mode 1: records measurements for each rising transition to the next falling one.

Mode 2 – Low Time Pulse Measurement (FIFO Buffer)

Timing measurements record the time interval (in 10 µs ticks) from a pair of transitions.



Pulse Low, Mode 2: records the interval from each falling edge to the next rising edge.

Mode 3 – Transition Timestamp of All Rising Edges (FIFO Buffer)

Rising Edge time stamps from 100 kHz, 32-bit counter will be sequentially available and stored in the FIFO buffer.

Note: In this example, four counter values at the rising edge transitions are recorded to the FIFO: 0x344321, 0x344999, 0x345011, 0x345689, etc.

Delta of 0x678 = 1656 counts, or 16.56 ms interval between pulses.

Mode 4 – Transition Timestamp of All Falling Edges (FIFO Buffer)

Falling Edge time stamps from 100 kHz, 32-bit counter will be sequentially available and stored in the FIFO buffer.

Mode 5 – Transition Timestamp of All Edges (FIFO Buffer)

Rising and Falling Edge time stamps from 100 kHz, 32-bit counter will be sequentially available and stored in the FIFO buffer.

Note: In this example, all edges time stamp. Four counter values at the transitions are recorded to the FIFO: 0x344321, 0x344999, 0x345011, 0x345689, etc.

Delta of 0x33C = 828 counts, or 8.28 ms interval between pulses.

Mode 6 – Rising Edge Transition Counter

When selected, the rising edge count will be available from the count register at the FIFO read address. The counter is reset via user command. 32-bit count range to 2^{32}.

Mode 7 – Falling Edge Transition Counter

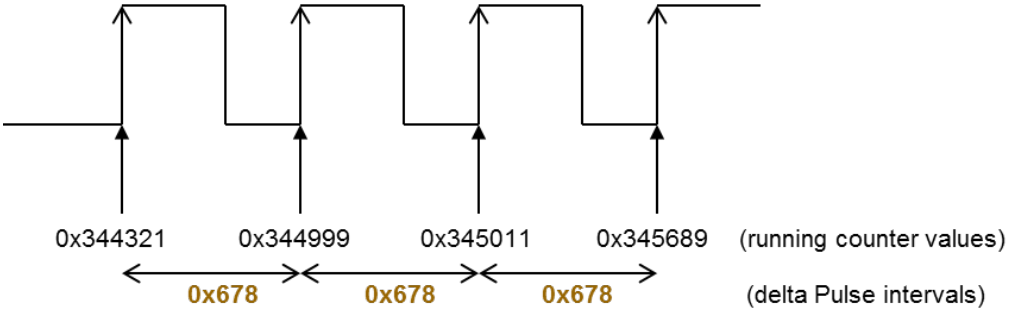
When selected, falling edge count will be available from the count register at the FIFO read address. The counter is reset via user command. 32-bit count range to 2^{32}.

Mode 8 – Rising and Falling Edge Transition Counter

When selected, cumulative edge counts will be available from the count register at the FIFO read address. The counter is reset via user command. 32-bit count range to 2^{32}.

Mode 9 - Period Measurement

Timing measurements record the intervals from pulse-to-pulse in 10 µs ticks (delta timestamp).



Note: In Period Measurement mode, the same three pulse-to-pulse interval values as calculated in the timestamp measurement would be directly recorded to the FIFO.

Mode 10 - Frequency Measurement

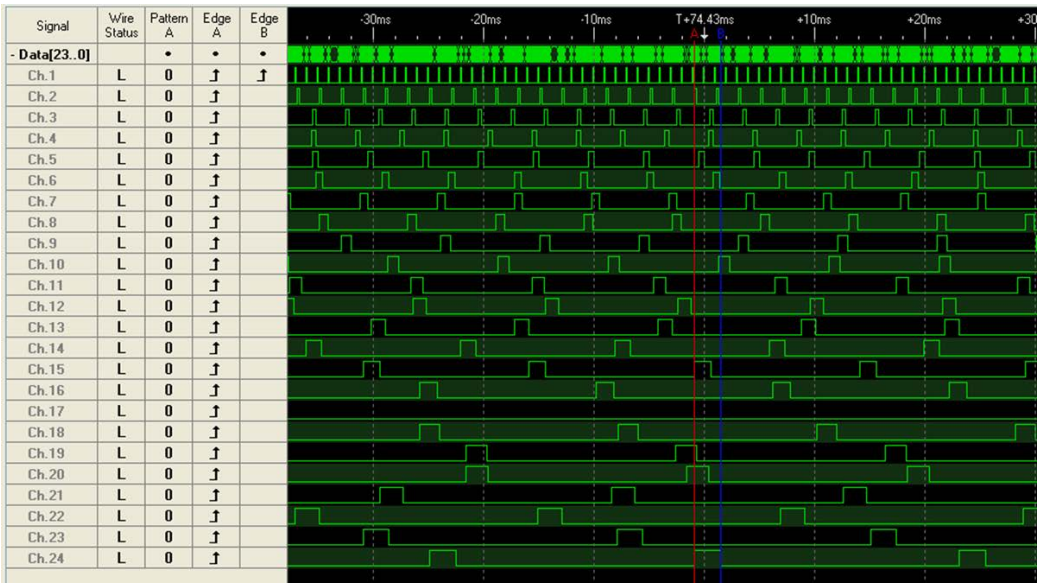
Enables frequency measurement, which will be available and stored in the FIFO buffer. Frequency measurement correlates to/utilizes a programmable time interval, which is programmed in the *Period* register. Direct readout of frequency is available when the interval is set to one second.

Output Modes

There are three Output modes, which include a standard output mode, two PWM outputs and a Pattern Generator Output mode.

Mode 32 (0x20) – PWM Continuous Output Mode

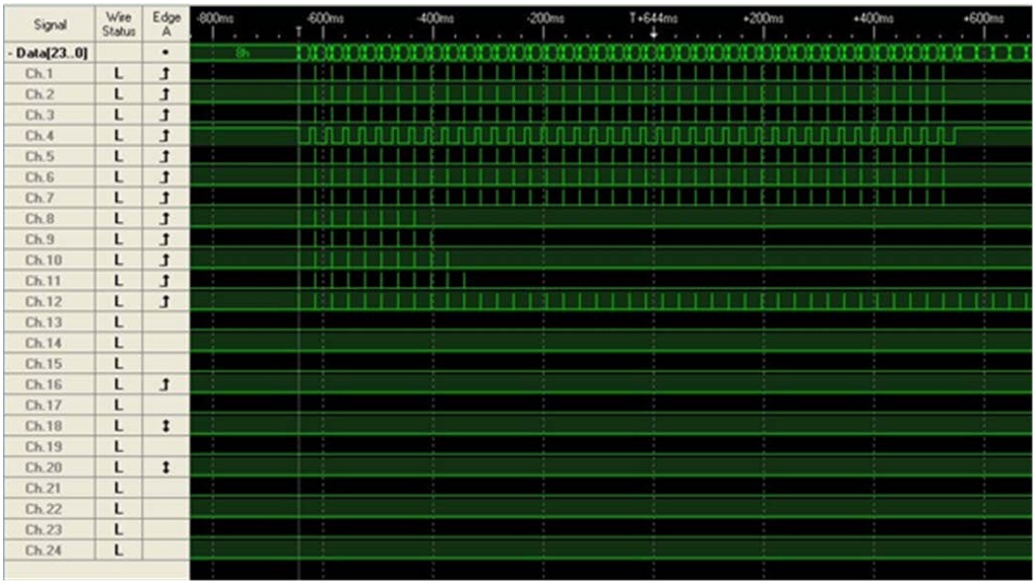
In the sample shown below, each of the 24 channels has been set up with incrementing periods and pulse widths, running in continuous mode. Timing is asynchronous to each channel, but is very precise and with low jitter. In this mode, the configured PWM output is enabled and disabled with the *Start Output/Measure Enable* register.



Continuous Output Mode (Mode 32)

Mode 33 (0x21) - PWM Burst

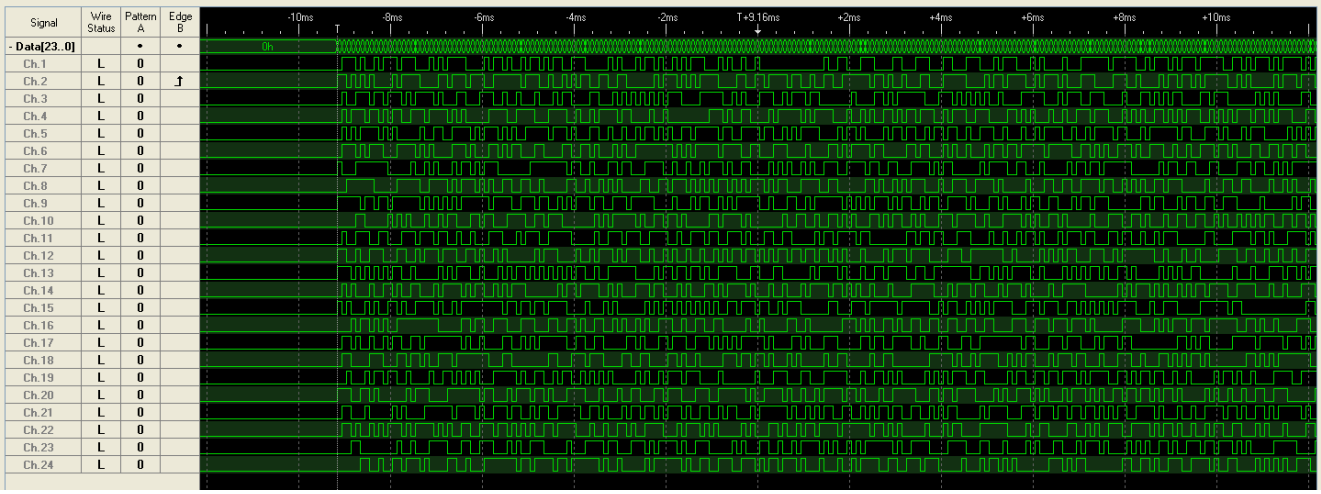
Repeats the pulse based on programmed Period and Pulse Width “n” times as programmed in the *Number of Cycles* register.



Burst Mode (Mode 33) Programmed for “n” Number of Cycles

Mode 34 (0x22) – Pattern Generator Output

Outputs all mode selected channels based on the pattern programmed in the *Pattern RAM* register. The output rate is set in the *Pattern RAM Period* register. The output is a cyclic transmission of a 2^{16} deep X 24 bit pattern array at configurable pattern intervals with 10 µs resolution. Pattern output may be stopped and resumed at the same point in the cycle. The following shows an arbitrary output of patterns as displayed on 24 channels of a logic analyzer. Each vertical column represents one 24-bit pattern of the 2^{16} pattern array.



Pattern Data Output (Mode 34)

Mode Select

Function: This register provides selection of 13 different modes: Inputs 1-10; Outputs 32-34. See the following table for a brief description of each mode.

Type: binary word (32-bit)

Data Range: 1-10; 32-34

Read/Write: R/W

Initialized Value: 0

Operational Settings: Modes 0 through 10, 32, 33 and 34 are selectable for each channel. Writing a **0** will return that channel to normal operation.

Mode #	Hex	Description
1	0x0001	**Measure "High" time**: Write a 1 to the *Start Output/Measure Enable* register to enable measurement of the I/O state "High" time. It will not be measured if the bit is not set for that channel, i.e. **0**. If a **1** is written to enable measurement on a channel while that channel's I/O state is **1,** then the internal counter will begin to count upon begin enabled.
2	0x0002	**Measure "Low" time**: Write a 1 to the *Start Output/Measure Enable* register to enable measurement of the I/O state "Low time". It will not be measured if the bit is not set for that channel. If a **1** is written to enable measurement on a channel while that channel's I/O state is **0,** then the internal counter will begin to count upon being enabled.
3	0x0003	**Time-stamp of all rising edges:** Write a 1 to the *Start Output/Measure Enable* register and the timestamp counter will begin to count. A low-to-high transition on that channel will store the timestamp at the time of the transition in the FIFO. If that channel is then disabled by writing a **0**, the timestamp counter will pause and any low-to-high transitions of the I/O state will not trigger FIFO storage. Write any value to the *Reset Timer* register to reset the timestamp counter.
4	0x0004	**Time-stamp of all falling edges**: Write a 1 to the *Start Output/Measure Enable* register and the timestamp counter will begin to count. A high-to-low transition on that channel will store the timestamp at the time of the transition in the FIFO. If that channel is then disabled by writing a **0**, the timestamp counter will pause and any high-to-low transitions of the I/O state will not trigger a FIFO storage. Write any value to the *Reset Timer* register to reset the timestamp counter.
5	0x0005	**Time-stamp of all edges**: Write a 1 to the *Start Output/Measure Enable* register and the timestamp counter will begin to count. Any low-to-high or high-to-low transition on that channel will store the timestamp at the time of the transition in the FIFO. If that channel is then disabled by writing a **0**, the timestamp counter will pause and any low-to-high or high-to-low transitions of the I/O state will not trigger FIFO storage. Write any value to the *Reset Timer* register to reset the timestamp counter.
6	0x0006	**Count total number of rising edges (until FIFO reset):** Write a 1 to the *Start Output/Measure Enable* register to begin tracking any low-to-high transition of that channel's I/O state will increment the counter by one. If a **0** is written in the register for that channel, the count will not increment on any transitions. Write any value to the *Reset Timer* register to reset the counter.
7	0x0007	**Count total number of falling edges (until FIFO reset)**: Write a 1 to the *Start Output/Measure Enable* register to begin tracking any high-to-low transition of that channel's I/O state will increment the counter by one. If a **0** is written in the register for that channel, the count will not increment on any transitions. Write any value to the *Reset Timer* register to reset the counter.
8	0x0008	**Count total number of all edges (until FIFO reset)**: Write a 1 to the *Start Output/Measure Enable* register to begin tracking any low-to-high transition or high-to-low transition of that channel's I/O state will increment the counter by one. If a **0** is written in the register for that channel, the count will not increment on any transitions. Write any value to the *Reset Timer* register to reset the counter.

Mode #	Hex	Description
9	0x0009	**Measure period from rising edge (L-H transition) to next rising edge**: The first low-to-high transition of any enabled channel will start the counter. The next low-to-high transition will store the count in the FIFO, reset the counter, and begin the count again. This will repeat. After the waveform on the input has finished, write any value to the *Reset Timer* to reset it to zero.
10	0x000A	**Measure frequency**: The first low-to-high transition of any enabled channel will start the PWM Period counter. The counter will be incremented for every low-to-high transition that occurs within the defined period. Once the period counter reaches zero, the number of low-to-high transitions counted will be stored in FIFO and the process will restart. Write any value to the *Reset Timer* to reset it to zero.
32	0x20	**PWM – output continuously:** Will continuously (repeat) the pulse based on programmed *Period* and *Pulse Width registers.* Write a **1** to output the continuous waveform programed in the *Period* and *Pulse Width* registers. Write a **0** to disable the output.
33	0x21	**PWM – output "n" times** Will repeat the pulse based on programmed *Period* and *Pulse Width* "n" times as programmed in the *Number of Cycles* register. Write a **1** to output the number of pulses written in the *Number of Cycles* register with the period and pulse width written in the *Period* and *Pulse Width* registers. Once the programmed number of pulses that was written to the register has been outputted, a **0** will be written back to the register for the channel that was enabled (self-clearing).
34	0x22	**Output pattern data held in RAM:** Outputs all mode selected channel(s) based on the pattern programmed in RAM. The output rate is set in the *Pattern RAM Period* register. The *Pattern RAM Start Address* register will determine where the pattern RAM output will begin when enabled. The *Pattern RAM End Address* register will determine where the pattern RAM output will end when enabled. After the pattern is outputted, it will loop back to the start address. Writing a 0x1 to the control register will loop the pattern continuously. While looping continuously, a 0x0 can be written to stop the output and bring the pattern back to the start address or a 0x5 can be written to pause the output wherever it may be in the pattern. Writing a 0x1 when the pattern is paused will resume the pattern at the same spot. Writing a 0x3 to the control register will burst the pattern from the start address to the end address for N number of times. N is determined by the value written in the *Pattern RAM Period* register. The *Pattern RAM Period* register determines how long the each address data will be output for. In other words, it is the time it takes for the output to change to the next address.

Notes:

	Input
	Output
1	Mode(s) 1-10: FIFO storage occurs at 10 µs intervals (unless otherwise specified)
2	Mode(s) 7- 9: Applies to measurement "count" edges – the "count" is provided/updated at 8ns intervals in the first element of the FIFO only (no FIFO 'storage" – first element is dynamically updated).
3	Mode 10 (Measure frequency): In this mode, the captured FIFO data is essentially the number of transitions measured within a given user specified time interval (specified/programmed in the *Pulse Width* register). From this, the user calculates frequency by [FIFO Data (# of transitions) / Pulse Width], or, simply program the *Pulse Width* register to a time interval of 1 second, which then FIFO Data (# of transitions) directly correlates to measured frequency (Hz).

Start Output/Measure Enable

Function:

Output Modes: When the Mode Select register is programmed for PWM output modes (Modes 32 & 33), the Start Output/Measure Enable register is used to start the channel outputs.

Input Modes: When the Mode Select register is programmed for input modes (Modes 1-10), the Start Output/Measure Enable register is used to start measurement.

Type: binary word (32-bit)

Data Range: 0x0000 0000 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: The channel(s) output is based on the pattern preset in the programmed pulse characteristic registers: *Period*, *Pulse Width* and *Output Polarity*. If the *Mode Select* register is set to Mode 33, the number of pulses is controlled by the *Number of Cycles* register.

Reset Timer

Function: Resets Timer to default value.

Type: binary word (32-bit)

Data Range: 0x0000 0000 to 0x0000 FFFF

Read/Write: W

Initialized Value: 0

Operational Settings: Writing any value to this register resets the Timer to default value. Applicable to Modes 3 through 10. See *Mode Select* register.

Notes: Resetting timers will also retrigger the FIFO store mechanism to trigger or restart the FIFO on the next valid low-to-high transition detected.

FIFO Operations/Functions

There is an independent FIFO (1024 32-bit words deep) for each channel allocated for use when the *Mode Select* register is programmed for the appropriate mode (applies to Modes 1-10).

Read FIFO/Read Count

Function: Depends upon *Mode Select* register setting.

Read FIFO: Provides stored data dependent on the input channel(s) mode selected. Applicable to Modes 1 through 5, 9 and 10. See *Mode Select* register.

Read Count: Applicable to Modes 6, 7 and 8. See *Mode Select* register.

Type: binary word (32-bit)

Data Range: 0x0000 0000 to 0xFFFF FFFF

Read/Write: R

Initialized Value: 0

Operational Settings: The available data in the FIFO buffer can be retrieved, one word at a time (32-bits), from the identified memory/register address.

Note

The *Read FIFO* and *Read Count* functions share a register. They are mutually exclusive in that depending upon the setting of the *Mode Select* register, either one or the other will become active.

Read FIFO Count

Function: Reads the number of 32-bit words stored in FIFO for each channel.

Type: binary word (32-bit)

Data Range: Any value

Read/Write: R/W

Initialized Value: 0

Operational Settings: Mode Select register set for Modes 1-10.

Read FIFO Status

Function: Provides a real-time status of the following conditions:

- FIFO empty
- FIFO full
- Almost Empty
- Almost Full

Type: binary word (32-bit)

Data Range: 0x0000 0000 to 0x4

Read/Write: R

Initialized Value: 0

Operational Settings: See table below.

Read FIFO Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Allocation
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	**#W**	**#W**	**#W**	**#W**	Allocation
X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	D=DATA BIT

D0 – Full

D1 – Almost Full

D2 – Almost Empty

D3 - Empty

Reset FIFO

Function: Resets measurement FIFO (only) to zero. Applicable to Modes 1 through 5, 9 and 10. See *Mode Select* register.

Type: binary word (32-bit)

Data Range: Any value

Read/Write: W

Initialized Value: 0

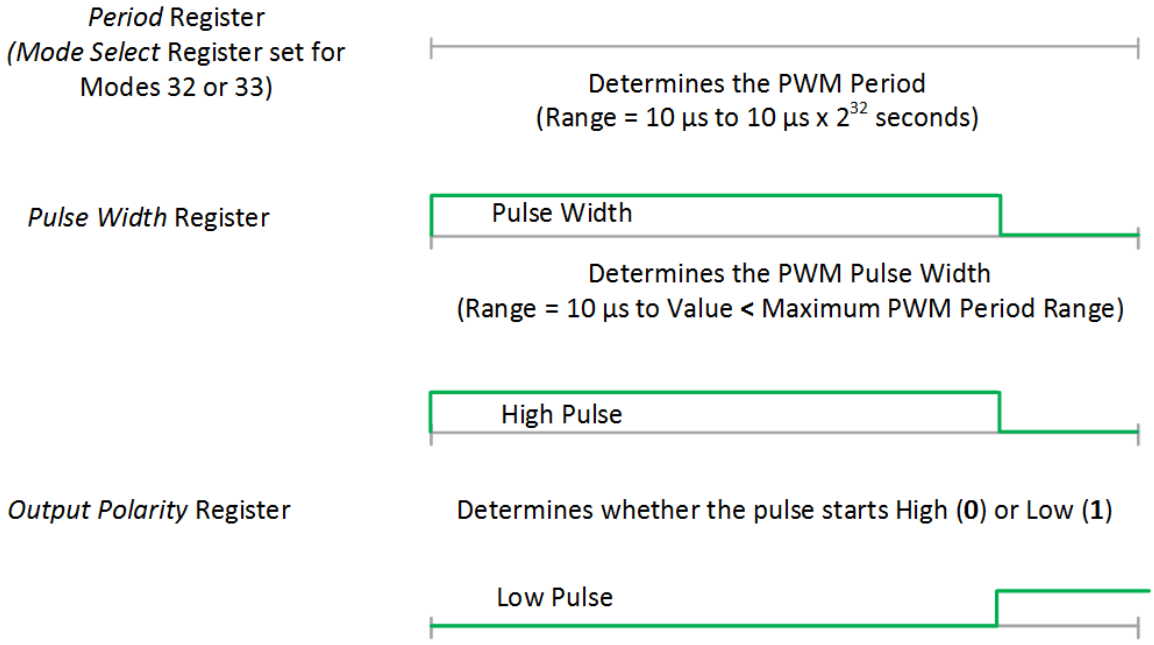
Operational Settings: The act of writing any value to this register will apply the reset.

PWM Operations/Functions

Unless otherwise specified, PWM operations and functions apply to channels when the *Mode Select* register is set for Modes 32 & 33.

Period

The Period register works in conjunction with the Pulse Width, Output Select, Number of Cycles and Start Output/Measure Enable registers to configure PWM output. See Configuring PWM Output figure below. It is also used for Period and Frequency measurement.



Configuring PWM Output

Function: When the *Mode Select* register is programmed for PWM output modes (Modes 32 & 33), the PWM Period is based on the programmed value set in this register.

Type: binary word (32-bit)

Data Range: 0x0000 0002 to 0xFFFF FFFE

Read/Write: R/W

Initialized Value: 0

Operational Settings: *Mode Select* register is set to Mode 32 or 33, the *Period* register is used to program the desired channel PWM output pulse period. Enter the desired PWM pulse period (LSB=@ 10 µs; valid entries are: 16 ns to 34.36 sec.).

Note: Programmed PWM Period must be greater than the value set in the *Pulse Width* register.

Pulse Width

Function:

When the *Mode Select* register is programmed for PWM output modes (Modes 32 & 33), the *Pulse Width* register is used to program the desired channel(s) PWM Pulse Width "ON" time. See Configuring PWM Output figure.

When the *Mode Select* register is programmed for frequency measurement (Mode 10), the *Pulse Width* register is used to program the Timebase for the desired channel(s).

Type: binary word (32-bit)

Data Range: 0x0000 0001 to 0xFFFF FFFE

Read/Write: R/W

Initialized Value: 0

Operational Settings:

Applied to Mode(s) 32 & 33: Enter the desired PWM Pulse Width (LSB=@ 10 µs; valid entries from 10 µs to @ 10 µs to 10 µs x 232 sec). Used in conjunction with the *Period* register.

Note: Programmed PWM Pulse Width must be **less than** the value set in the *Period* register.

Applied to Mode 10: For channel(s) with functions that rely on frequency measurement, the *Pulse Width* register is used to program the desired channel "Timebase" for the frequency measurement transition count period of time.

Note: There may be an initial "low" level output delay based on the Period time before the initial pulse is output.

Number of Cycles

Function: When *Mode Select* register is programmed for Mode 33, the *Number of Cycles* register is used to program the number of times to repeat the pulse.

Type: binary word (32-bit)

Data Range: 0x0000 0001 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Pulse is determined and used in conjunction with the *Period* and *Pulse Width* registers. Enter the desired Number of Cycles.

Note: If continuous pulse generation is desired, select Mode 32.

Pattern Generator Operations/Functions

Applies to channels set for Output mode 34 on the *Mode Select* register. There is an allocated RAM data pattern 64K deep RAM location range, bit-mapped per channel that can be used for multichannel pulse pattern generation. Each channel, when programmed for Mode 34, is bit-mapped (LSB = Ch1) and when triggered (timers are reset), will sequentially output the programmed RAM pattern at the rate programmed in the *Pattern RAM Period* register.

Pattern RAM Period

Function: Programs the desired channel output pattern rate.

Type: binary word (32-bit)

Data Range: 0x0000 0001 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Enter the desired Pattern Generator RAM period (LSB=@ 10 µs).

Pattern RAM Start Address

Function: Programs the starting address for the Pattern Generator.

Type: binary word (32-bit)

Data Range: 0x40000 to 0x7FFFC

Read/Write: R/W

Initialized Value: 0

Operational Settings: Output rate is determined by the rate programmed in the Pattern RAM Period register. Write a “0x1” to start the RAM pattern output; write a “0x0” to stop the RAM pattern output.

Pattern RAM Start Address																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	24	23	22	21	20	19	18	17	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Pattern RAM End Address

Function: Programs the ending address for the Pattern Generator. There are 32K address locations from 0x40000 to 0x7FFFC

Type: binary word (32-bit)

Data Range: 0x40000 to 0x7FFFC

Read/Write: R/W

Initialized Value: 0

Operational Settings: NA

Pattern RAM End Address																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	24	23	22	21	20	19	18	17	Channel
X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Pattern RAM Number of Cycles

Function: Program the number of times to repeat the pattern.

Type: binary word (32-bit)

Data Range: 0x0000 0001 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Programmable from 1 to 2^{32} cycles.

Pattern RAM Control

Function: Control the RAM data pattern.

Type: binary word (32-bit)

Data Range: N/A

Read/Write: W

Initialized Value: 0

Operational Settings: The *Pattern RAM Start Address* register determines where the pattern RAM output will begin when enabled. The *Pattern RAM End Address* register determines where the pattern RAM output will end when enabled. After the pattern at the pattern end address is outputted, it will loop back to the start address.

Pattern RAM Control																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	24	23	22	21	20	19	18	17	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Notes: Write the following values to the register to perform each function.

Bit	Function
D0	Pattern Looping: This bit will enable or disable continuous pattern looping. Write **0x1** to enable and **0x0** to disable the pattern.
D1	Burst Mode: Write **0x3** will burst the pattern from the start address to the end address for N number of times. N is determined by the value written in the *Pattern RAM Number of Cycles* register.
D2	Pause: Write **0x5** to pause the pattern when enabled.
D3	Rising Edge External Trigger Enable: Uses Channel 1 as the input. Write **0xA** to enable pattern burst on a rising edge.
D4	Falling Edge External Trigger Enable: Uses Channel 1 as the input. Write **0x12** to enable pattern burst on a falling edge.

Output Polarity

Function: When the *Mode Select* register is programmed for PWM output modes (Modes 32 & 33), the *Output Polarity* programs the PWM Pulse Period to start either High (**0**) or Low (**1**).

Type: binary word (32-bit)

Data Range: 0x0000 0000 to 0x0000 FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Applies to Modes 32 and 33. The *Output Polarity* register is used to program the start "level" (or state) of the PWM Pulse Period. The default is ON (High), which is set when the PWM Polarity bit is **0.** The PWM start level channel(s) output will be High for the initial start of the period. See Configuring PWM Output figure. The time is defined by the *Period* and *Pulse Width* registers. The remainder of the PWM Period time will be "low" defined by the [PWM Period - PWM Pulse Width]. If the PWM Polarity bit is set to **1**, the PWM start level will be "low" for the programmed PWM Pulse Width and the remainder of the PWM Period time will be "high" defined by the [PWM Period – PWM Pulse Width]. Bit mapped per channel.

Note: There may be an initial "low" level output delay based on the Period time before the initial pulse is output.

Output Polarity																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Function Register Map

0x1000	Switch Control	R/W
0x1004	Read I/O	R
0x1008	Overcurrent Reset	R/W
0x1010	Switch State	R
0x100C	Open Circuit Detection (*1)	R/W
0x2F00	Start Output/Measure Enable	R/W
0x2F04	Reset Timer	W
0x2F08	Reset FIFO	W
0x2F0C	Output Polarity	R/W
0x2F10	Pattern RAM Control	W
0x2F14	Pattern RAM Start Address	R/W
0x2F18	Pattern RAM End Address	R/W
0x2F1C	Pattern RAM Period	R/W
0x2F20	Pattern RAM Num of Cycles	R/W

0x2000	Voltage Reading (Sampled) Ch.1	R
0x2080	Voltage Reading (Sampled) Ch.2	R
0x2100	Voltage Reading (Sampled) Ch.3	R
0x2180	Voltage Reading (Sampled) Ch.4	R
0x2200	Voltage Reading (Sampled) Ch.5	R
0x2280	Voltage Reading (Sampled) Ch.6	R
0x2300	Voltage Reading (Sampled) Ch.7	R
0x2380	Voltage Reading (Sampled) Ch.8	R
0x2400	Voltage Reading (Sampled) Ch.9	R
0x2480	Voltage Reading (Sampled) Ch.10	R
0x2500	Voltage Reading (Sampled) Ch.11	R
0x2580	Voltage Reading (Sampled) Ch.12	R
0x2600	Voltage Reading (Sampled) Ch.13	R
0x2680	Voltage Reading (Sampled) Ch.14	R
0x2700	Voltage Reading (Sampled) Ch.15	R
0x2780	Voltage Reading (Sampled) Ch.16	R

0x2004	Voltage Reading (Averaged) Ch.1	R
0x2084	Voltage Reading (Averaged) Ch.2	R
0x2104	Voltage Reading (Averaged) Ch.3	R
0x2184	Voltage Reading (Averaged) Ch.4	R
0x2204	Voltage Reading (Averaged) Ch.5	R
0x2284	Voltage Reading (Averaged) Ch.6	R
0x2304	Voltage Reading (Averaged) Ch.7	R
0x2384	Voltage Reading (Averaged) Ch.8	R
0x2404	Voltage Reading (Averaged) Ch.9	R
0x2484	Voltage Reading (Averaged) Ch.10	R
0x2504	Voltage Reading (Averaged) Ch.11	R
0x2584	Voltage Reading (Averaged) Ch.12	R
0x2604	Voltage Reading (Averaged) Ch.13	R
0x2684	Voltage Reading (Averaged) Ch.14	R
0x2704	Voltage Reading (Averaged) Ch.15	R
0x2784	Voltage Reading (Averaged) Ch.16	R

(*1) Note: A. Open Circuit Detection enhanced feature; introduced/available on EAR FPGA rev. 3; top-boards rev D (DOM @ 10/2016)

0x 2008	Current Reading (Sampled) Ch.1	R
0x 2088	Current Reading (Sampled) Ch.2	R
0x 2108	Current Reading (Sampled) Ch.3	R
0x 2188	Current Reading (Sampled) Ch.4	R
0x 2208	Current Reading (Sampled) Ch.5	R
0x 2288	Current Reading (Sampled) Ch.6	R
0x 2308	Current Reading (Sampled) Ch.7	R
0x 2388	Current Reading (Sampled) Ch.8	R
0x 2408	Current Reading (Sampled) Ch.9	R
0x 2C88	Current Reading (Sampled) Ch.10	R
0x 2508	Current Reading (Sampled) Ch.11	R
0x 2588	Current Reading (Sampled) Ch.12	R
0x 2608	Current Reading (Sampled) Ch.13	R
0x 2688	Current Reading (Sampled) Ch.14	R
0x 2708	Current Reading (Sampled) Ch.15	R
0x 2788	Current Reading (Sampled) Ch.16	R

0x 200C	Current Reading (Averaged) Ch.1	R
0x 208C	Current Reading (Averaged) Ch.2	R
0x 210C	Current Reading (Averaged) Ch.3	R
0x 218C	Current Reading (Averaged) Ch.4	R
0x 220C	Current Reading (Averaged) Ch.5	R
0x 228C	Current Reading (Averaged) Ch.6	R
0x 230C	Current Reading (Averaged) Ch.7	R
0x 238C	Current Reading (Averaged) Ch.8	R
0x 240C	Current Reading (Averaged) Ch.9	R
0x 248C	Current Reading (Averaged) Ch.10	R
0x 250C	Current Reading (Averaged) Ch.11	R
0x 258C	Current Reading (Averaged) Ch.12	R
0x 260C	Current Reading (Averaged) Ch.13	R
0x 268C	Current Reading (Averaged) Ch.14	R
0x 270C	Current Reading (Averaged) Ch.15	R
0x 278C	Current Reading (Averaged) Ch.16	R

0x2010	Debounce Time Ch.1	R/W
0x2090	Debounce Time Ch.2	R/W
0x2110	Debounce Time Ch.3	R/W
0x2190	Debounce Time Ch.4	R/W
0x2210	Debounce Time Ch.5	R/W
0x2290	Debounce Time Ch.6	R/W
0x2310	Debounce Time Ch.7	R/W
0x2390	Debounce Time Ch.8	R/W
0x2410	Debounce Time Ch.9	R/W
0x2C90	Debounce Time Ch.10	R/W
0x2510	Debounce Time Ch.11	R/W
0x2590	Debounce Time Ch.12	R/W
0x2610	Debounce Time Ch.13	R/W
0x2690	Debounce Time Ch.14	R/W
0x2710	Debounce Time Ch.15	R/W
0x2790	Debounce Time Ch.16	R/W

0x2014	Max. High Threshold Ch.1	R/W
0x2094	Max. High Threshold Ch.2	R/W
0x2114	Max. High Threshold Ch.3	R/W
0x2194	Max. High Threshold Ch.4	R/W
0x2214	Max. High Threshold Ch.5	R/W
0x2294	Max. High Threshold Ch.6	R/W
0x2314	Max. High Threshold Ch.7	R/W
0x2394	Max. High Threshold Ch.8	R/W
0x2414	Max. High Threshold Ch.9	R/W
0x2494	Max. High Threshold Ch.10	R/W
0x2514	Max. High Threshold Ch.11	R/W
0x2594	Max. High Threshold Ch.12	R/W
0x2614	Max. High Threshold Ch.13	R/W
0x2694	Max. High Threshold Ch.14	R/W
0x2714	Max. High Threshold Ch.15	R/W
0x2794	Max. High Threshold Ch.16	R/W

0x2018	Upper Threshold Ch.1	R/W
0x2098	Upper Threshold Ch.2	R/W
0x2118	Upper Threshold Ch.3	R/W
0x2198	Upper Threshold Ch.4	R/W
0x2218	Upper Threshold Ch.5	R/W
0x2298	Upper Threshold Ch.6	R/W
0x2318	Upper Threshold Ch.7	R/W
0x2398	Upper Threshold Ch.8	R/W
0x2418	Upper Threshold Ch.9	R/W
0x2C98	Upper Threshold Ch.10	R/W
0x2518	Upper Threshold Ch.11	R/W
0x2598	Upper Threshold Ch.12	R/W
0x2618	Upper Threshold Ch.13	R/W
0x2698	Upper Threshold Ch.14	R/W
0x2718	Upper Threshold Ch.15	R/W
0x2798	Upper Threshold Ch.16	R/W

0x201C	Lower Threshold Ch.1	R/W
0x209C	Lower Threshold Ch.2	R/W
0x211C	Lower Threshold Ch.3	R/W
0x219C	Lower Threshold Ch.4	R/W
0x221C	Lower Threshold Ch.5	R/W
0x229C	Lower Threshold Ch.6	R/W
0x231C	Lower Threshold Ch.7	R/W
0x239C	Lower Threshold Ch.8	R/W
0x241C	Lower Threshold Ch.9	R/W
0x249C	Lower Threshold Ch.10	R/W
0x251C	Lower Threshold Ch.11	R/W
0x259C	Lower Threshold Ch.12	R/W
0x261C	Lower Threshold Ch.13	R/W
0x269C	Lower Threshold Ch.14	R/W
0x271C	Lower Threshold Ch.15	R/W
0x279C	Lower Threshold Ch.16	R/W

0x2020	Min. Low Threshold Ch.1	R/W
0x20A0	Min. Low Threshold Ch.2	R/W
0x2120	Min. Low Threshold Ch.3	R/W
0x21A0	Min. Low Threshold Ch.4	R/W
0x2220	Min. Low Threshold Ch.5	R/W
0x22A0	Min. Low Threshold Ch.6	R/W
0x2320	Min. Low Threshold Ch.7	R/W
0x23A0	Min. Low Threshold Ch.8	R/W
0x2420	Min. Low Threshold Ch.9	R/W
0x2CA0	Min. Low Threshold Ch.10	R/W
0x2520	Min. Low Threshold Ch.11	R/W
0x25A0	Min. Low Threshold Ch.12	R/W
0x2620	Min. Low Threshold Ch.13	R/W
0x26A0	Min. Low Threshold Ch.14	R/W
0x2720	Min. Low Threshold Ch.15	R/W
0x27A0	Min. Low Threshold Ch.16	R/W

0x2024	Overcurrent Value Ch.1	R/W
0x20A4	Overcurrent Value Ch.2	R/W
0x2124	Overcurrent Value Ch.3	R/W
0x21A4	Overcurrent Value Ch.4	R/W
0x2224	Overcurrent Value Ch.5	R/W
0x22A4	Overcurrent Value Ch.6	R/W
0x2324	Overcurrent Value Ch.7	R/W
0x23A4	Overcurrent Value Ch.8	R/W
0x2424	Overcurrent Value Ch.9	R/W
0x2CA4	Overcurrent Value Ch.10	R/W
0x2524	Overcurrent Value Ch.11	R/W
0x25A4	Overcurrent Value Ch.12	R/W
0x2624	Overcurrent Value Ch.13	R/W
0x26A4	Overcurrent Value Ch.14	R/W
0x2724	Overcurrent Value Ch.15	R/W
0x27A4	Overcurrent Value Ch.16	R/W

0x3000	Read FIFO/Read Count Ch.1	R
0x3080	Read FIFO/Read Count Ch.2	R
0x3100	Read FIFO/Read Count Ch.3	R
0x3180	Read FIFO/Read Count Ch.4	R
0x3200	Read FIFO/Read Count Ch.5	R
0x3280	Read FIFO/Read Count Ch.6	R
0x3300	Read FIFO/Read Count Ch.7	R
0x3380	Read FIFO/Read Count Ch.8	R
0x3400	Read FIFO/Read Count Ch.9	R
0x3480	Read FIFO/Read Count Ch.10	R
0x3500	Read FIFO/Read Count Ch.11	R
0x3580	Read FIFO/Read Count Ch.12	R
0x3600	Read FIFO/Read Count Ch.13	R
0x3680	Read FIFO/Read Count Ch.14	R
0x3700	Read FIFO/Read Count Ch.15	R
0x3780	Read FIFO/Read Count Ch.16	R

0x3004	Read FIFO Count Ch.1	R
0x3084	Read FIFO Count Ch.2	R
0x3104	Read FIFO Count Ch.3	R
0x3184	Read FIFO Count Ch.4	R
0x3204	Read FIFO Count Ch.5	R
0x3284	Read FIFO Count Ch.6	R
0x3304	Read FIFO Count Ch.7	R
0x3384	Read FIFO Count Ch.8	R
0x3404	Read FIFO Count Ch.9	R
0x3484	Read FIFO Count Ch.10	R
0x3504	Read FIFO Count Ch.11	R
0x3584	Read FIFO Count Ch.12	R
0x3604	Read FIFO Count Ch.13	R
0x3684	Read FIFO Count Ch.14	R
0x3704	Read FIFO Count Ch.15	R
0x3784	Read FIFO Count Ch.16	R

0x3008	Read FIFO Status Ch.1	R
0x3088	Read FIFO Status Ch.2	R
0x3108	Read FIFO Status Ch.3	R
0x3188	Read FIFO Status Ch.4	R
0x3208	Read FIFO Status Ch.5	R
0x3288	Read FIFO Status Ch.6	R
0x3308	Read FIFO Status Ch.7	R
0x3388	Read FIFO Status Ch.8	R
0x3408	Read FIFO Status Ch.9	R
0x3488	Read FIFO Status Ch.10	R
0x3508	Read FIFO Status Ch.11	R
0x3588	Read FIFO Status Ch.12	R
0x3608	Read FIFO Status Ch.13	R
0x3688	Read FIFO Status Ch.14	R
0x3708	Read FIFO Status Ch.15	R
0x3788	Read FIFO Status Ch.16	R

0x300C	Mode Ch.1	R/W
0x308C	Mode Ch.2	R/W
0x310C	Mode Ch.3	R/W
0x318C	Mode Ch.4	R/W
0x320C	Mode Ch.5	R/W
0x328C	Mode Ch.6	R/W
0x330C	Mode Ch.7	R/W
0x338C	Mode Ch.8	R/W
0x340C	Mode Ch.9	R/W
0x348C	Mode Ch.10	R/W
0x350C	Mode Ch.11	R/W
0x358C	Mode Ch.12	R/W
0x360C	Mode Ch.13	R/W
0x368C	Mode Ch.14	R/W
0x370C	Mode Ch.15	R/W
0x378C	Mode Ch.16	R/W

0x3010	Pulse Width Ch.1	R/W
0x3090	Pulse Width Ch.2	R/W
0x3110	Pulse Width Ch.3	R/W
0x3190	Pulse Width Ch.4	R/W
0x3210	Pulse Width Ch.5	R/W
0x3290	Pulse Width Ch.6	R/W
0x3310	Pulse Width Ch.7	R/W
0x3390	Pulse Width Ch.8	R/W
0x3410	Pulse Width Ch.9	R/W
0x3490	Pulse Width Ch.10	R/W
0x3510	Pulse Width Ch.11	R/W
0x3590	Pulse Width Ch.12	R/W
0x3610	Pulse Width Ch.13	R/W
0x3690	Pulse Width Ch.14	R/W
0x3710	Pulse Width Ch.15	R/W
0x3790	Pulse Width Ch.16	R/W

0x3014	Period Ch.1	R/W
0x3094	Period Ch.2	R/W
0x3114	Period Ch.3	R/W
0x3194	Period Ch.4	R/W
0x3214	Period Ch.5	R/W
0x3294	Period Ch.6	R/W
0x3314	Period Ch.7	R/W
0x3394	Period Ch.8	R/W
0x3414	Period Ch.9	R/W
0x3494	Period Ch.10	R/W
0x3514	Period Ch.11	R/W
0x3594	Period Ch.12	R/W
0x3614	Period Ch.13	R/W
0x3694	Period Ch.14	R/W
0x3714	Period Ch.15	R/W
0x3794	Period Ch.16	R/W

0x3018	Number of Cycles Ch.1	R/W
0x3098	Number of Cycles Ch.2	R/W
0x3118	Number of Cycles Ch.3	R/W
0x3198	Number of Cycles Ch.4	R/W
0x3218	Number of Cycles Ch.5	R/W
0x3298	Number of Cycles Ch.6	R/W
0x3318	Number of Cycles Ch.7	R/W
0x3398	Number of Cycles Ch.8	R/W
0x3418	Number of Cycles Ch.9	R/W
0x3498	Number of Cycles Ch.10	R/W
0x3518	Number of Cycles Ch.11	R/W
0x3598	Number of Cycles Ch.12	R/W
0x3618	Number of Cycles Ch.13	R/W
0x3698	Number of Cycles Ch.14	R/W
0x3718	Number of Cycles Ch.15	R/W
0x3798	Number of Cycles Ch.16	R/W

BIT

0x0800	BIT Dynamic Status	R
0x0804	BIT Latched Status	R/W
0x0808	BIT Interrupt Enable	R/W
0x080C	BIT Set Edge/Level Interrupt	R/W

Overcurrent

0x0810	Overcurrent Dynamic Status	R
0x0814	Overcurrent Latched Status	R/W
0x0818	Overcurrent Interrupt Enable	R/W
0x081C	Overcurrent Set Edge/Level Interrupt	R/W

Threshold

0x0820	Max. Hi Threshold Dynamic Status	R
0x0824	Max. Hi Threshold Latched Status	R/W
0x0828	Max. Hi Threshold Interrupt Enable	R/W
0x082C	Max. Hi Threshold Set Edge/Level Interrupt	R/W

0x0830	Min. Lo Threshold Dynamic Status	R
0x0834	Min. Lo Threshold Latched Status	R/W
0x0838	Min. Lo Threshold Interrupt Enable	R/W
0x083C	Min. Lo Threshold Set Edge/Level Interrupt	R/W

Mid-Range

0x0840	Mid-Range Dynamic Status	R
0x0844	Mid-Range Latched Status	R/W
0x0848	Mid-Range Interrupt Enable	R/W
0x084C	Mid-Range Set Edge/Level Interrupt	R/W

Transition

0x0850	Low-High Transition Dynamic Status	R
0x0854	Low-High Transition Latched Status	R/W
0x0858	Low-High Transition Interrupt Enable	R/W
0x085C	Low-High Transition Set Edge/Level Interrupt	R/W

0x0860	High-Low Transition Dynamic Status	R
0x0864	High-Low Transition Latched Status	R/W
0x0868	High-Low Transition Interrupt Enable	R/W
0x086C	High-Low Transition Set Edge/Level Interrupt	R/W

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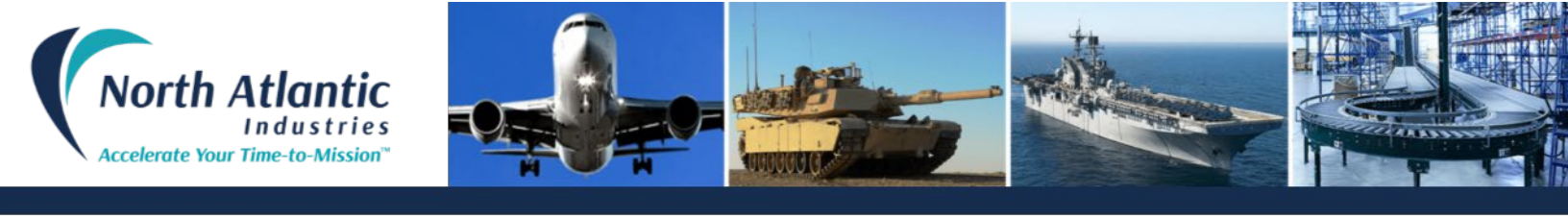

Enhanced Discrete I/O, Digital I/O Functionality

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	7/10/2019	Initial release	GC
A1	5/06/2020	ECO C07548: Module manuals updated for formatting consistency. No technical or specification updates.	MC

Table of Contents

1 Enhanced Input/Output Functionality Capability

The Enhanced Input/Output Functionality Capability is available on the following modules:

- Differential Transceiver Modules
  - DF2 – 16 Channels Differential I/O
- Discrete I/O Modules
  - DT4 – 24 Channels, Programmable for either input or output, output up to 500 mA per channel from an applied external 3 – 60 VCC source.
  - DT5 – 16 Channels, Programmable for either input voltage measurements (±80 V) or as a bi-directional current switch (up to 500 mA per channel).
  - DT6 – 4 Channels, Programmable for either input voltage measurements (±100 V) or as a bi-directional current switch (up to 3 A per channel).
- TTL/CMOS Modules
  - TL2, TL4, TL6 and TL8 – 24 Channels, Programmable for either input or output.

2 Principle of Operation

The modules listed in section 1 provide enhanced input and output mode functionality. For incoming signals (inputs), the enhanced modes include Pulse, Frequency and Period measurements. For outputs, the enhanced modes include PWM (Pulse Width Modulation) and Pattern Generation.

2.1 Input Modes

All input modes may be configured with debounce capability. Debounce capability allows configurable filtering of noisy signals and transients. Each channel may be set to an individual debounce time value. When a debounce time is set to a non-zero value, the signal reading after a transition must remain at the same level for the debounce interval before it is propagated through, otherwise it is rejected.

The waveform shown in Figure 1 will be used to illustrate the behavior for each input mode.

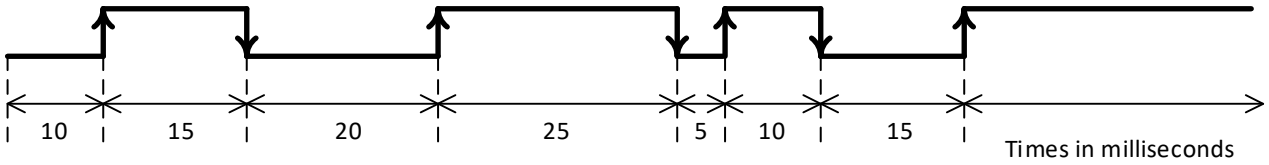

Figure 1 - Incoming Signal Example Used to illustrate Input Modes

2.1.1 Pulse Measurements

There are two Pulse Measurements features available – High Time Pulse Measurements and Low Time Pulse Measurements. The Pulse Measurement data is stored in the FIFO Buffer.

2.1.1.1 High Time Pulse Measurements

In this input mode, the data in the FIFO buffer is the measurement for each rising transition to the next falling one. Timing measurements record the time interval (in 10 µs ticks) from a pair of transitions.

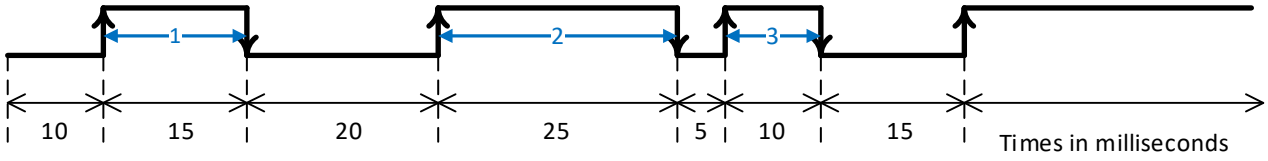

Figure 2 - High Time Pulse Measurement Input Mode

For this example, the *FIFO Word Count* register will be set to 3 and the *FIFO Buffer Data* register will contain the following three values (counts of 10 µs):

1. 1500 (0x0000 05DC)
2. 2500 (0x0000 09C4)
3. 1000 (0x0000 03E8)

Time Interval	Calculations	High Time Pulse Measurements
1	1500 counts * 10 µsec = 15000 µsec = 15.0 msec	15.0 msec
2	2500 counts * 10 µsec = 25000 µsec = 25.0 msec	25.0 msec
3	1000 counts * 10 µsec = 10000 µsec = 10.0 msec	10.0 msec

2.1.1.2 Low Time Pulse Measurements

In this mode, the data in the FIFO buffer is the measurement for each falling edge to the next rising edge. Timing measurements record the time interval (in 10 µs ticks) from a pair of transitions.

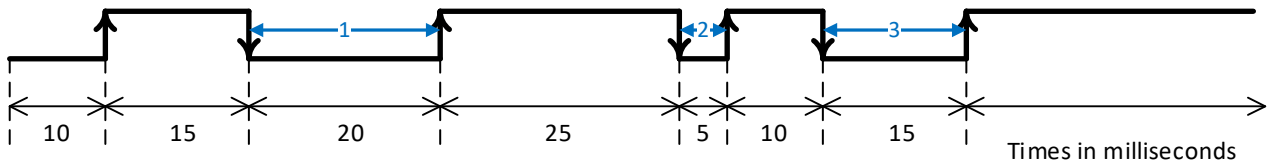

Figure 3 - Low Time Pulse Measurement Input Mode

For this example, the *FIFO Word Count* register will be set to 3 and the *FIFO Buffer Data* register will contain the following three values (counts of 10 µs):

1. 2000 (0x0000 07D0)
2. 500 (0x0000 01F4)
3. 1500 (0x0000 05DC)

Time Interval	Calculations	Low Time Pulse Measurements
1	2000 counts * 10 µsec = 20000 µsec = 20.0 msec	20.0 msec
2	500 counts * 10 µsec = 5000 µsec = 5.0 msec	5.0 msec
3	1500 counts * 10 µsec = 15000 µsec = 15.0 msec	15.0 msec

2.1.2 Transition Timestamps

There are three Transition Timestamp Measurements features available – Transition Timestamp for All Rising Edges, Transition Timestamp for All Falling Edges, and Transition Timestamp for All Edges. The Transition Timestamps Measurement data are store in the FIFO Buffer.

2.1.2.1 Transition Timestamp of All Rising Edges

In this mode, the data in the FIFO buffer is the Rising Edge Timestamp. The timestamp is a 32-bit counter that is incremented at the rate of 100 kHz (in other words, counter is incremented every 10 µsec). The timestamp is can be reset by the application at any time.

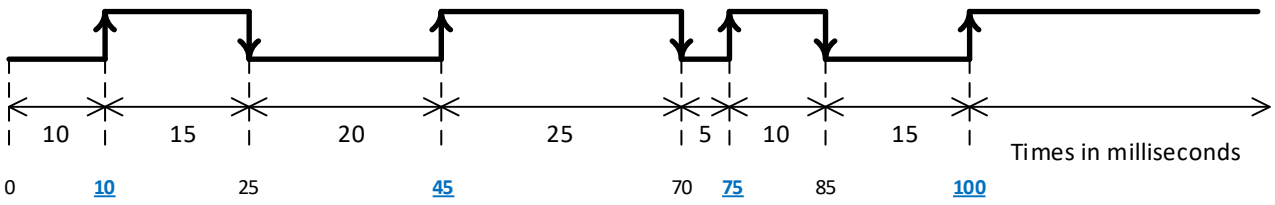

Figure 4 - Transition Timestamp of All Rising Edges Input Mode

For this example, the *FIFO Word Count* register will be set to 4 and the *FIFO Buffer Data* register will contain the following four values (counts of 10 µs):

1. 1000 (0x0000 03E8)
2. 4500 (0x0000 1194)
3. 7500 (0x0000 1D4C)
4. 10000 (0x000 2710)

This data can be interpreted as follows:

Time Interval	Calculations	Time between rising edges
1 to 2	4500 – 1000 = 3500 counts = 3500 * 10 µsec = 35000 µsec = 35.0 msec	35.0 msec
2 to 3	7500 – 4500 = 3000 counts = 3000 * 10 µsec = 30000 µsec = 30.0 msec	30.0 msec
3 to 4	10000 – 7500 = 2500 counts = 2500 * 10 µsec = 25000 µsec = 25.0 msec	25.0 msec

2.1.2.2 Transition Timestamp of All Falling Edges

In this mode, the data in the FIFO buffer is the Falling Edge Timestamp. The timestamp is a 32-bit counter that is incremented at the rate of 100 kHz (in other words, counter is incremented every 10 µsec). The timestamp is can be reset by the application at any time.

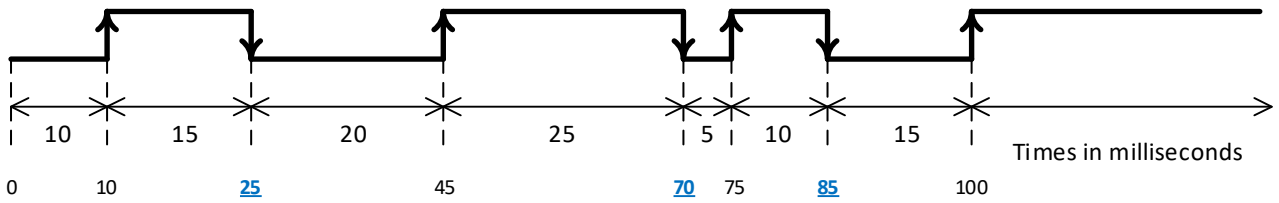

Figure 5 - Transition Timestamp of All Falling Edges Input Mode

For this example, the *FIFO Word Count* register will be set to 3 and the *FIFO Buffer Data* register will contain the following three values (counts of 10 µs):

1. 2500 (0x0000 09C4)
2. 7000 (0x0000 1B58)
3. 8500 (0x0000 2134)

This data can be interpreted as follows:

Time Interval	Calculations	Time between falling edges
1 to 2	7000 – 2500 = 4500 counts = 4500 * 10 µsec = 45000 µsec = 45.0 msec	45.0 msec
2 to 3	8500 – 7000 = 1500 counts = 1500 * 10 µsec = 15000 µsec = 15.0 msec	15.0 msec

2.1.2.3 Transition Timestamp of All Edges

In this mode, the data in the FIFO buffer is the Rising and Falling Edge Timestamp. The timestamp is a 32-bit counter that is incremented at the rate of 100 kHz (in other words, counter is incremented every 10 µsec). The timestamp is can be reset by the application at any time.

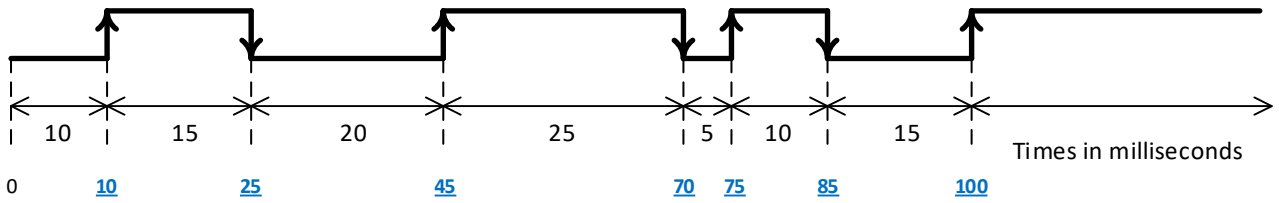

Figure 6 - Transition Timestamp for All Edges Input Mode

For this example, the *FIFO Word Count* register will be set to 7 and the *FIFO Buffer Data* register will contain the following seven values (counts of 10 µs):

1. 1000 (0x0000 03E8)

2. 2500 (0x0000 09C4)
3. 4500 (0x0000 1194)
4. 7000 (0x0000 1B58)
5. 7500 (0x0000 1D4C)
6. 8500 (0x0000 2134)
7. 10000 (0x000 2710)

This data can be interpreted as follows:

Time Interval	Calculations	Time between edges
1 to 2	2500 – 1000 = 1500 counts = 1500 * 10 µsec = 15000 µsec = 15.0 msec	15.0 msec
2 to 3	4500 – 2500 = 2000 counts = 2000 * 10 µsec = 20000 µsec = 20.0 msec	20.0 msec
3 to 4	7000 – 4500 = 2500 counts = 2500 * 10 µsec = 25000 µsec = 25.0 msec	25.0 msec
4 to 5	7500 – 7000 = 500 counts = 500 * 10 µsec = 5000 µsec = 5.0 msec	5.0 msec
5 to 6	8500 – 7500 = 1000 counts = 1000 * 10 µsec = 10000 µsec = 10.0 msec	10.0 msec
6 to 7	10000 – 8500 = 1500 counts = 1500 * 10 µsec = 15000 µsec = 15.0 msec	15.0 msec

2.1.3 Transition Counter

There are three Transition Counter features available – Rising Edge Transition Counter, Falling Edge Transition Counter and All Edge Transition Counter.

2.1.3.1 Rising Edges Transition Counter

In this mode, the count of the number of Rising Edges is recorded. The counter is a 32-bit counter. The counter is can be reset by the application at any time.

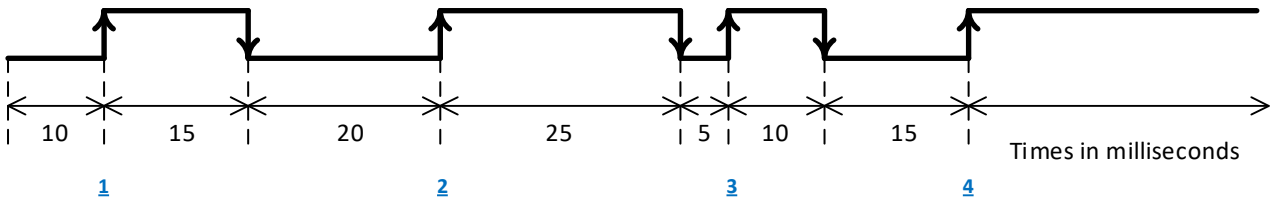

Figure 7 – Rising Edges Transition Counter Input Mode

For this example, the *Transition Count* register will be set to 4.

2.1.3.2 Falling Edges Transition Counter

In this mode, the count of the number of Falling Edges is recorded. The counter is a 32-bit counter. The counter is can be reset by the application at any time.

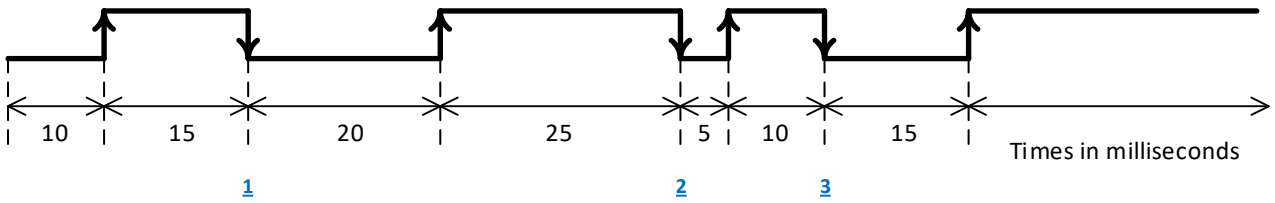

Figure 8 - Falling Edges Transition Counter Input Mode

For this example, the *Transition Count* register will be set to 3.

2.1.3.3 All Edges Transition Counter

In this mode, the count of the number of Rising and Falling Edges is recorded. The counter is a 32-bit counter. The counter is can be reset by the application at any time.

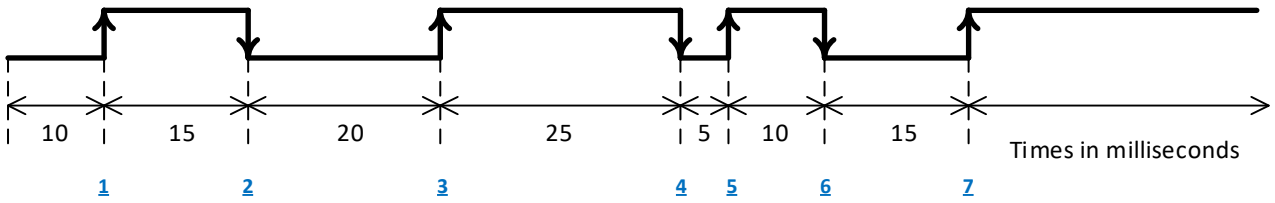

Figure 9 - All Edges Transition Counter Input Mode

For this example, the *Transition Count* register will be set to 7.

2.1.4 Period Measurement

In this input mode, the data in the FIFO buffer is the measurement for each rising edge transition to the next rising edge transition. Timing measurements record the time interval (in 10 µs ticks).

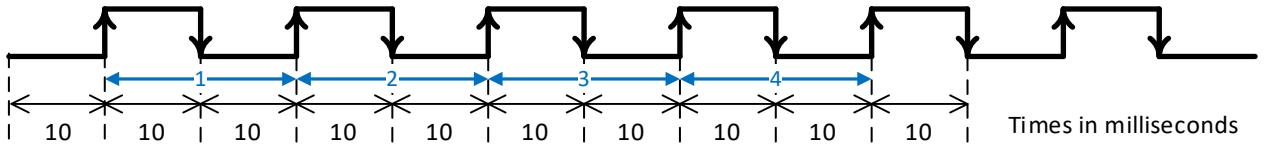

Figure 10 - Period Measurement Input Mode

For this example, the *FIFO Word Count* register will be set to 4 and the *FIFO Buffer Data* register will contain the following three values (counts of 10 µs):

1. 2000 (0x0000 07D0)
2. 2000 (0x0000 07D0)
3. 2000 (0x0000 07D0)
4. 2000 (0x0000 07D0)

Time Interval	Calculations	Period Measurements
1	2000 counts * 10 µsec = 20000 µsec = 20.0 msec	20.0 msec
2	2000 counts * 10 µsec = 20000 µsec = 20.0 msec	20.0 msec
3	2000 counts * 10 µsec = 20000 µsec = 20.0 msec	20.0 msec
4	2000 counts * 10 µsec = 20000 µsec = 20.0 msec	20.0 msec

2.1.5 Frequency Measurement

In this input mode, the data in the FIFO buffer is the number of rising edge transitions for the programmable time interval programmed in the *Frequency Measurement Period* register.

For this example, set the *Frequency Measurement Period* register = 4000 (4000 * 10 µs = 40000 µs = 40 msec).

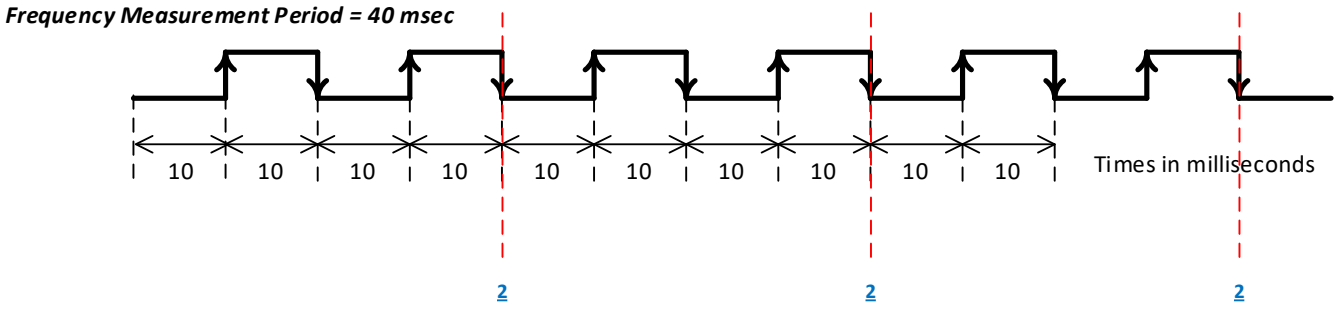

Figure 11 - Frequency Measurement Input Mode

For this example, the *FIFO Word Count* register will be set to 3 and the *FIFO Buffer Data* register will contain the following three values (number of rising edges:

1. 2 (0x0000 0002)
2. 2 (0x0000 0002)
3. 2 (0x0000 0002)

Time Interval	Calculations	Frequency Measurements
1	2 counts/40 msec = 2 counts/0.04 seconds = 50 Hz	50 Hz
2	2 counts/40 msec = 2 counts/0.04 seconds = 50 Hz	50 Hz
3	2 counts/40 msec = 2 counts/0.04 seconds = 50 Hz	50 Hz

2.2 Output Modes

There are three Enhanced Output Functionality modes: two PWM outputs and one Pattern Generator Output mode.

2.2.1 PWM Output

There are two PWM output modes, PWM Continuous and PWM Burst. The PWM timing is very precise with low jitter. In PWM Output mode, the *Mode Select* register is set to either "PWM Continuous or PWM Burst". The value written to the *PWM Period* register specifies the period to output the PWM signal, the value written to the *PWM Pulse Width* register specifies the time for the "ON" state, and the value written to the *PWM Output Polarity* register specifies the initial edge of the output. For PWM Burst mode, the *PWM Number of Cycles* register specifies the number of cycles to output the signal. Note, there may be an initial "OFF" state level delay based on the Period time before the initial pulse is output.

2.2.1.1 PWM Continuous

Figure 12 and Figure 13 illustrate the PWM Continuous Output signal, one configured with PWM Output Polarity = Positive (0) and one configured with PWM Output Polarity = Negative (1). The configured PWM output is enabled and disabled with the *Enable Measurements/Outputs* register.

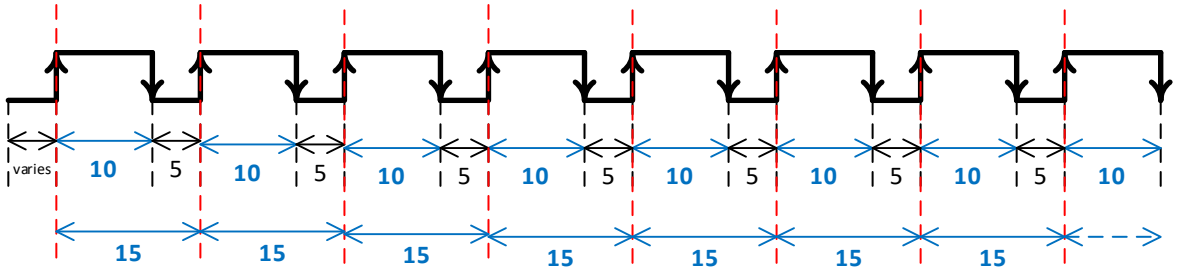

Figure 12 - PWM Continuous Output
(*PWM Period* = 15 msec, *PWM Pulse Width* = 10 msec, *PWM Output Polarity* = Positive (0))

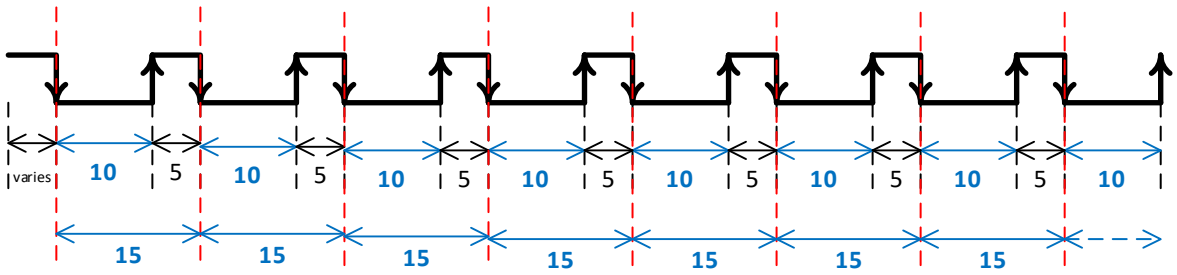

Figure 13 - PWM Continuous Output
(*PWM Period* = 15 msec, *PWM Pulse Width* = 10 msec, *PWM Output Polarity* = Negative (1))

2.2.1.2 PWM Burst

Figure 14 and Figure 15 illustrate the PWM Burst Output signal with the PWM Number of Cycles = 5 pulses, one configured with PWM Output Polarity = Positive (0) and one configured with PWM Output Polarity = Negative (1). The configured PWM output is enabled with the *Enable Measurements/Outputs* register. Once the number of pulses that were requested is outputted, the value in the *Enable Measurements/Outputs* register will be reset (self-clearing) to allow for the output to be re-enabled.

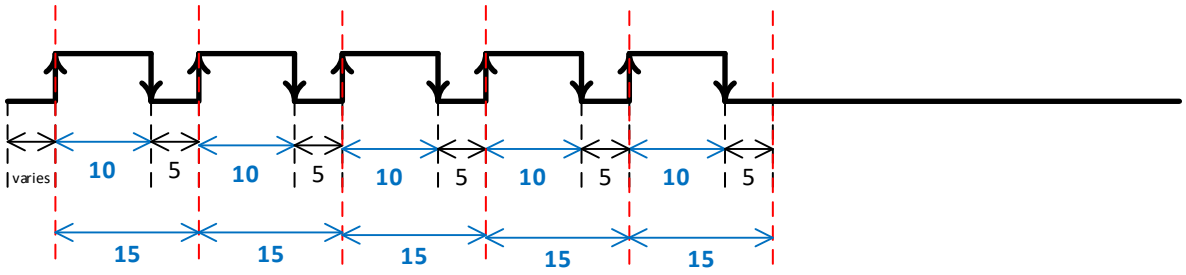

Figure 14 - PWM Burst Output
(*PWM Period* = 15 msec, *PWM Pulse Width* = 10 msec, *PWM Output Polarity* = Positive (0), *PWM Number of Cycles* = 5)

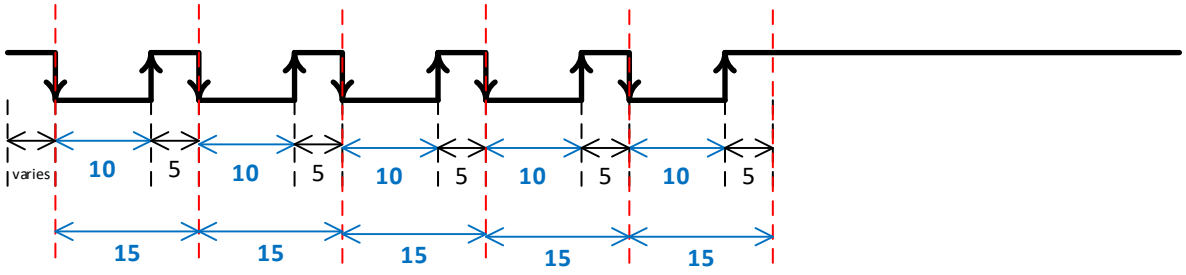

Figure 15 - PWM Burst Output
(*PWM Period* = 15 msec, *PWM Pulse Width* = 10 msec, *PWM Output Polarity* = Negative (1)), *PWM Number of Cycles* = 5)

2.2.2 Pattern Generator

For the Pattern Generator mode, there is 64K block of unsigned 32-bit words allocated to specify the data pattern for the output channels. The data in each 32-bit word is bit-mapped per channel. The *Pattern RAM Start Address* and *Pattern RAM End Address* registers specify the starting and ending address in the 64K block to use as the data to output for each channel configured for Pattern Generator mode. The *Pattern RAM Period* register specifies the pattern rate. The *Pattern RAM Control* and *Pattern RAM Number of Cycles* control the Pattern Generator output – Continuous, Burst with a specified number of cycles, Pause, or External Trigger from input from Channel 1. Note, when *any* channel is configured for *External Trigger Pattern Generator* mode, *Channel 1 must be set as an input*.

Figure 16 illustrates the output of the 24 channels for the DT4 module all configured in Pattern Generator mode.

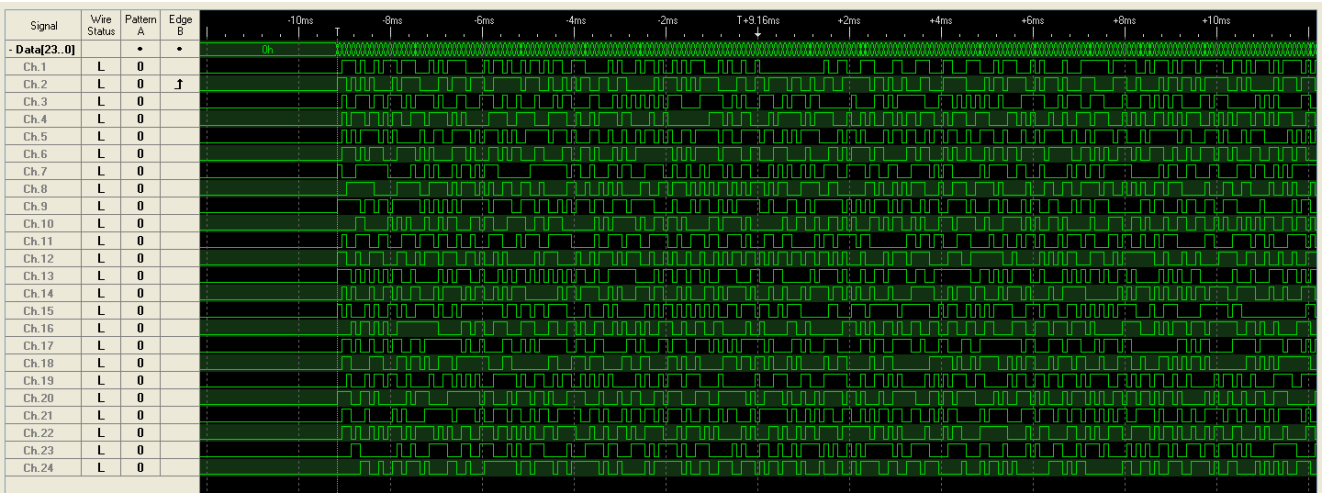

Figure 16 - Pattern Generator

3 Register Descriptions

The register descriptions provide the register name, Type, Data Range, Read or Write information, Initialized Value, and a description of the function.

3.1 Enhanced I/O Functionality Registers

The modules listed in section 1 provide enhanced input and output mode functionality. The *Mode Select* and *Enable Output/Measurement* registers are general control registers for the different enhanced input and output modes.

3.1.1 Mode Select

Function: Configures the Enhanced Functionality Modes to apply to the channel.

Type: unsigned binary word (32-bit)

Data Range: See table

Read/Write: R/W

Initialized Value: 0

Operational Settings: It is important that the channel is correctly configured to either input or output in the *Input/Output Format* registers to correspond to the Enhanced Functionality Mode selected. Setting a **0** to this register will configure that channel to normal operation.

Mode Select Value (Decimal)	Mode Select Value (Hexadecimal)	Description
0	0x0000 0000	Enhanced Functionality Disabled
Input Enhanced Functionality Mode		
1	0x0000 0001	High Time Pulse Measurements
2	0x0000 0002	Low Time Pulse Measurements
3	0x0000 0003	Transition Timestamp of All Rising Edges
4	0x0000 0004	Transition Timestamp of All Falling Edges
5	0x0000 0005	Transition Timestamp of All Edges
6	0x0000 0006	Rising Edges Transition Counter
7	0x0000 0007	Falling Edges Transition Counter
8	0x0000 0008	All Edges Transition Counter
9	0x0000 0009	Period Measurement
10	0x0000 000A	Frequency Measurement
Output Enhanced Functionality Mode		
32	0x0000 0020	PWM Continuous
33	0x0000 0021	PWM Burst
34	0x0000 0022	Pattern Generator

3.1.2 Enable Measurements/Outputs

Function: Enables/starts the measurements or outputs based on the *Mode Select* for the channel.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0x00FF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Setting the bit for the associated channel to a "1" will start the measurement or output depending on the *Mode Select* configuration for that channel. Setting the bit for the associated channel to "0" will stop the measurements/outputs.

Enable Measurements/Outputs															
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

3.1.3 Input Modes Registers

After configuring the *Mode Select* register, write a "1" to the *Reset Timer/Counter* register resets the channel's timestamp and counter used for input modes. Write a "1" to the *Enable Measurements/Outputs* register to begin the measurement of the input signal. Write a "0" to the *Enable Measurements/Outputs* register to stop the measurement of the input signal. The data can be read either while the measurements are being made on input signals or after stopping the measurements.

3.1.3.1 Reset Timer/Counter

Function: Resets the measurement timestamp and counter for the channel.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0x00FF FFFF

Read/Write: W

Initialized Value: 0

Operational Settings: Setting the bit for the associated channel to a "1" will:

- reset the timestamp used for the Pulse Measurements mode (1-2), Transition Timestamp mode (3-5), and Period Measurement mode (9) and Frequency Measurement mode (10)
- reset the counter used for Transition Counter mode (6-8)

Reset Timer/Counter															
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

3.1.3.2 FIFO Registers

The FIFO registers are used for the following input modes:

- Pulse Measurements mode (1-2)
- Transition Timestamp mode (3-5)
- Period Measurement mode (9)
- Frequency Measurement mode (10)

3.1.3.2.1 FIFO Buffer Data

Function: The data stored in the FIFO Buffer Data is dependent on the input mode.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0xFFFF FFFF
Read/Write: R
Initialized Value: N/A
Operational Settings: Refer to examples in section 2.1.

3.1.3.2.2 FIFO Word Count

Function: This is a counter that reports the number of 32-bit words stored in the FIFO buffer.
Type: unsigned binary word (32-bit)
Data Range: 0 – 255 (0x0000 0000 to 0x0000 00FF)
Read/Write: R
Initialized Value: 0
Operational Settings: Every time a read operation is made from the *FIFO Buffer Data* register, the value in the *FIFO Word Count* register will be decremented by one. The maximum number of words that can be stored in the FIFO is 255.

FIFO Word Count															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

3.1.3.2.3 Clear FIFO

Function: Clears FIFO by resetting the *FIFO Word Count* register.
Type: unsigned binary word (32-bit)
Data Range: 0 or 1
Read/Write: W
Initialized Value: N/A
Operational Settings: Write a **1** to resets the *Words in FIFO* to zero; *Clear FIFO* register does not clear data in the buffer. A read to the buffer data will give “aged” data.

D31-D1	Reserved. Set to 0
D0	Set to 1 to reset the *FIFO Word Count* value to zero.

Clear FIFO															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**D**

3.1.3.2.4 FIFO Status

Function: Sets the corresponding bit associated with the FIFO status type; there is a separate register for each channel.
Type: unsigned binary word (32-bit)

Data Range: See table
Read/Write: R
Initialized Value: 0

Description		
D31-D4	Reserved	Set to 0
D3	Empty	Set to 1 when FIFO Word Count = 0
D2	Almost Empty	Set to 1 when FIFO Word Count <= 63 (25%)
D1	Almost Full	Set to 1 when FIFO Word Count >= 191 (75%)
D0	Full	Set to 1 when FIFO Word Count = 255

FIFO Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**

3.1.3.3 Transition Count Registers

The *Transition Count* register are used for the following input modes:

- Transition Counter mode (6-8)

3.1.3.3.1 Transition Count

Function: Contains the count of the transitions depending on the configuration in the *Mode Select* register – Rising Edges, Falling Edges or All Edges.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0xFFFF FFFF

Read/Write: R

Initialized Value: 0

Operational Settings: Refer to examples in section 2.1.3.

3.1.3.4 Frequency Measurement Registers

For the Frequency Measurement mode, the period to perform the frequency measurements must be specified in the *Frequency Measurement Period* register.

3.1.3.4.1 Frequency Measurement Period

Function: When the *Mode Select* register is programmed for Frequency Measurement mode (10), the value in the Frequency Measurement Period is used as the time interval for counting the number of rising edge transitions within that interval.

Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Set the Frequency Measurement Period (LSB = 10 µs). Refer to examples in section 2.1.5.

3.1.4 Output Modes Registers

After configuring the *Mode Select* register, write a "1" to the *Enable Measurements/Outputs* register to outputting the signal. Write a "0" to the *Enable Measurements/Outputs* register to stop the output signal.

3.1.4.1 PWM Registers

The *PWM Period, PWM Pulse Width* and *PWM Output Polarity* registers configure the PWM output signal. When the *Mode Select* register is configured for PWM Burst mode, the *PWM Number of Cycles* register is used to specify the number of cycles to repeat for the burst.

3.1.4.1.1 PWM Period

Function: When the *Mode Select* register is programmed for PWM Continuous or PWM Burst mode (32-33), the value in the PWM Period is used as the time interval for outputting the PWM signal.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0001 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Set the PWM Period (LSB = 10 µs). The PWM Period must be greater than the value set in the *PWM Pulse Width* register. Refer to examples in section 2.2.1.

3.1.4.1.2 PWM Pulse Width

Function: When the *Mode Select* register is programmed for PWM Continuous or PWM Burst mode (32-33), the value in the PWM Pulse Width is used as the time interval of the "ON" state for outputting the PWM signal.

Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Set the PWM Pulse Width (LSB = 10 µs). The PWM Pulse Width must be less than the value set in the *PWM Pulse Width* register. Refer to examples in section 2.2.1.

3.1.4.1.3 PWM Output Polarity

Function: When the *Mode Select* register is programmed for PWM Continuous or PWM Burst mode (32-33), the value in the *PWM Output Polarity* is used to specify whether the PWM output signal starts with a rising edge (Positive (**0**)), or a falling edge (Negative (**1**)).

Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0x00FF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: The *PWM Output Polarity* register is used to program the starting edge of the PWM Pulse Period (rising or falling). When the PWM output Polarity is set to Positive (0), the output will start with a rising edge, when it's set to Negative (1), the output will start with a falling edge. The default is Positive (0), which is set when the PWM Polarity bit is **0.** Refer to examples in section 2.2.1.

PWM Output Polarity															
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

3.1.4.1.4 PWM Number of Cycles

Function: When the *Mode Select* register is programmed for PWM Burst mode (33), the value in the *PWM Number of Cycles* is used to specify the number of times to repeat the PWM output signal.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0001 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Set the number of times to output the PWM signal. Refer to examples in section 2.2.1.

3.1.4.2 Pattern Generator Registers

The *Pattern RAM* registers are a 64K block of unsigned 32-bit words allocated to specify the data pattern for the output channels. The *Pattern RAM Start Address*, *Pattern RAM End Address*, *Pattern RAM Period* and *Pattern RAM Control* registers configure the Pattern Generator output signals. When the *Pattern RAM Control* register is configured for Burst, the *Pattern RAM Number of Cycles* specify the number of cycles to repeat the pattern for the burst.

3.1.4.2.1 Pattern RAM

Function: Pattern Generator Memory Block from 0x40000 to 0x7FFFC.

Type: unsigned binary word (32-bit)

Address Range: 0x0000 0000 to 0x00FF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: 64K block of unsigned 32-bit words. The data in each 32-bit word is bit-mapped per channel.

Pattern RAM															
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	Ch24	Ch23	Ch22	Ch21	Ch20	Ch19	Ch18	Ch17
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Ch16	Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

3.1.4.2.2 Pattern RAM Start Address

Function: When the *Mode Select* register is programmed for Pattern Generator mode (34), the *Pattern RAM Start Address* register specifies the starting address within the *Pattern RAM* block registers to use for the output.

Type: unsigned binary word (32-bit)

Data Range: 0x0004 0000 to 0x0007 FFFC

Read/Write: R/W

Initialized Value: 0

Operational Settings: The value in the *Pattern RAM Start Address* must be less than the value in the *Pattern RAM End Address*.

Pattern RAM Start Address															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

3.1.4.2.3 Pattern RAM End Address

Function: When the *Mode Select* register is programmed for Pattern Generator mode (34), the *Pattern RAM End Address* register specifies the end address within the *Pattern RAM* block registers to use for the output.

Type: unsigned binary word (32-bit)

Data Range: 0x40000 to 0x7FFFC

Read/Write: R/W

Initialized Value: 0

Operational Settings: The value in the *Pattern RAM End Address* must be greater than the value in the *Pattern RAM Start Address*.

Pattern RAM End Address															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

3.1.4.2.4 Pattern RAM Period

Function: When the *Mode Select* register is programmed for Pattern Generator mode (34), the value in the *Pattern RAM Period* is used as the time interval for outputting the Pattern Generator signals.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0001 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: Set the Pattern RAM Period (LSB = 10 µs).

3.1.4.2.5 Pattern RAM Control

Function: When the *Mode Select* register is programmed for Pattern Generator mode (34), the value in the *Pattern RAM Control* is used to control the outputting of the Pattern Generator signals.

Type: unsigned binary word (32-bit)

Data Range: See table

Read/Write: R/W

Initialized Value: 0

Operational Settings: Configures the Patter Generator for Continuous, Burst with a specified number of cycles, Pause, or External Trigger from input from Channel 1. Note, when *any* channel is configured for *External Trigger Pattern Generator* mode, *Channel 1 must be set as an input*.

Bits	Description
D31-D5	Reserved. Set to 0
D4	Falling Edge External Trigger – Channel 1 used as the input for the trigger
D3	Rising Edge External Trigger – Channel 1 used as the input for the trigger
D2	Pause
D1	Burst Mode – value in *Pattern RAM Number of Cycles* register defines number of cycles to output
D0	Enable Pattern Generator

Values	Description
0x0000	Disable Pattern Generator, Continuous Mode, No External Trigger
0x0001	Enable Pattern Generator, Continuous Mode, No External Trigger
0x0002	Disable Pattern Generator, Burst Mode, No External Trigger
0x0003	Enable Pattern Generator, Burst Mode, No External Trigger
0x0005	Enable Pattern Generator, Continuous Mode, Pause, No External Trigger
0x0007	Enable Pattern Generator, Burst Mode, Pause, No External Trigger
0x0008	Disable Pattern Generator, Continuous Mode, Rising External Trigger
0x0009	Enable Pattern Generator, Continuous Mode, Rising External Trigger
0x000A	Disable Pattern Generator, Burst Mode, Rising External Trigger
0x000B	Enable Pattern Generator, Burst Mode, Rising External Trigger
0x000D	Enable Pattern Generator, Continuous Mode, Pause, Rising External Trigger
0x000F	Enable Pattern Generator, Burst Mode, Pause, Rising External Trigger
0x1000	Disable Pattern Generator, Continuous Mode, Falling External Trigger
0x1001	Enable Pattern Generator, Continuous Mode, Falling External Trigger
0x1002	Disable Pattern Generator, Burst Mode, Falling External Trigger
0x1003	Enable Pattern Generator, Burst Mode, Falling External Trigger
0x1005	Enable Pattern Generator, Continuous Mode, Pause, Falling External Trigger
0x1007	Enable Pattern Generator, Burst Mode, Pause, Falling External Trigger
0x0004, 0x0006, 0x000C, 0x000E, 0x1004, 0x1006, 0x1008-0x100F	Invalid

Pattern RAM Control															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**

3.1.4.2.6 Pattern RAM Number of Cycles

Function: When the *Mode Select* register is programmed for Pattern Generator mode (34) and the *Pattern RAM Control* register is set for Burst mode, the value in the *Pattern RAM Number of Cycles* is used to specify the number of times to repeat the pattern output signal.

Type: unsigned binary word (32-bit)
Data Range: 0x0000 0001 to 0xFFFF FFFF
Read/Write: R/W
Initialized Value: 0
Operational Settings: Set the number of times to output the pattern.

4 Function Register Map

Key: ***Bold Italic = Configuration/Control***

Bold Underline = Status

*When an event is detected, the bit associated with the event is set in this register and will remain set until the user clears the event bit. Clearing the bit requires writing a 1 back to the specific bit that was set when read (i.e. write-1-to-clear, writing a '1' to a bit set to '1' will set the bit to '0').

4.1 Enhanced I/O Functionality Registers

0x300C	***Mode Select Ch 1***	R/W
0x308C	***Mode Select Ch 2***	R/W
0x310C	***Mode Select Ch 3***	R/W
0x318C	***Mode Select Ch 4***	R/W
0x320C	***Mode Select Ch 5***	R/W
0x328C	***Mode Select Ch 6***	R/W
0x330C	***Mode Select Ch 7***	R/W
0x338C	***Mode Select Ch 8***	R/W
0x340C	***Mode Select Ch 9***	R/W
0x348C	***Mode Select Ch 10***	R/W
0x350C	***Mode Select Ch 11***	R/W
0x358C	***Mode Select Ch 12***	R/W

0x360C	***Mode Select Ch 13***	R/W
0x368C	***Mode Select Ch 14***	R/W
0x370C	***Mode Select Ch 15***	R/W
0x378C	***Mode Select Ch 16***	R/W
0x380C	***Mode Select Ch 17***	R/W
0x388C	***Mode Select Ch 18***	R/W
0x390C	***Mode Select Ch 19***	R/W
0x398C	***Mode Select Ch 20***	R/W
0x3A0C	***Mode Select Ch 21***	R/W
0x3A8C	***Mode Select Ch 22***	R/W
0x3B0C	***Mode Select Ch 23***	R/W
0x3B8C	***Mode Select Ch 24***	R/W

0x2000	***Enable Measurements/Outputs***	R/W

4.1.1 Input Modes Registers

0x2004	***Reset Timer/Counter***	W

4.1.1.1 FIFO Registers

0x3000	**FIFO Buffer Data Ch 1**	R
0x3080	**FIFO Buffer Data Ch 2**	R
0x3100	**FIFO Buffer Data Ch 3**	R
0x3180	**FIFO Buffer Data Ch 4**	R
0x3200	**FIFO Buffer Data Ch 5**	R
0x3280	**FIFO Buffer Data Ch 6**	R
0x3300	**FIFO Buffer Data Ch 7**	R
0x3380	**FIFO Buffer Data Ch 8**	R
0x3400	**FIFO Buffer Data Ch 9**	R
0x3480	**FIFO Buffer Data Ch 10**	R
0x3500	**FIFO Buffer Data Ch 11**	R
0x3580	**FIFO Buffer Data Ch 12**	R

0x3600	**FIFO Buffer Data Ch 13**	R
0x3680	**FIFO Buffer Data Ch 14**	R
0x3700	**FIFO Buffer Data Ch 15**	R
0x3780	**FIFO Buffer Data Ch 16**	R
0x3800	**FIFO Buffer Data Ch 17**	R
0x3880	**FIFO Buffer Data Ch 18**	R
0x3900	**FIFO Buffer Data Ch 19**	R
0x3980	**FIFO Buffer Data Ch 20**	R
0x3A00	**FIFO Buffer Data Ch 21**	R
0x3A80	**FIFO Buffer Data Ch 22**	R
0x3B00	**FIFO Buffer Data Ch 23**	R
0x3B80	**FIFO Buffer Data Ch 24**	R

0x3004	FIFO Word Count Ch 1	R
0x3084	FIFO Word Count Ch 2	R
0x3104	FIFO Word Count Ch 3	R
0x3184	FIFO Word Count Ch 4	R
0x3204	FIFO Word Count Ch 5	R
0x3284	FIFO Word Count Ch 6	R
0x3304	FIFO Word Count Ch 7	R
0x3384	FIFO Word Count Ch 8	R
0x3404	FIFO Word Count Ch 9	R
0x3484	FIFO Word Count Ch 10	R
0x3504	FIFO Word Count Ch 11	R
0x3584	FIFO Word Count Ch 12	R

0x3604	FIFO Word Count Ch 13	R
0x3684	FIFO Word Count Ch 14	R
0x3704	FIFO Word Count Ch 15	R
0x3784	FIFO Word Count Ch 16	R
0x3804	FIFO Word Count Ch 17	R
0x3884	FIFO Word Count Ch 18	R
0x3904	FIFO Word Count Ch 19	R
0x3984	FIFO Word Count Ch 20	R
0x3A04	FIFO Word Count Ch 21	R
0x3A84	FIFO Word Count Ch 22	R
0x3B04	FIFO Word Count Ch 23	R
0x3B84	FIFO Word Count Ch 24	R

0x3008	FIFO Status Ch 1	R
0x3088	FIFO Status Ch 2	R
0x3108	FIFO Status Ch 3	R
0x3188	FIFO Status Ch 4	R
0x3208	FIFO Status Ch 5	R
0x3288	FIFO Status Ch 6	R
0x3308	FIFO Status Ch 7	R
0x3388	FIFO Status Ch 8	R
0x3408	FIFO Status Ch 9	R
0x3488	FIFO Status Ch 10	R
0x3508	FIFO Status Ch 11	R
0x3588	FIFO Status Ch 12	R

0x3608	FIFO Status Ch 13	R
0x3688	FIFO Status Ch 14	R
0x3708	FIFO Status Ch 15	R
0x3788	FIFO Status Ch 16	R
0x3808	FIFO Status Ch 17	R
0x3888	FIFO Status Ch 18	R
0x3908	FIFO Status Ch 19	R
0x3988	FIFO Status Ch 20	R
0x3A08	FIFO Status Ch 21	R
0x3A88	FIFO Status Ch 22	R
0x3B08	FIFO Status Ch 23	R
0x3B88	FIFO Status Ch 24	R

0x2008	***Reset FIFO***	W

4.1.1.2 Transition Count Registers

0x3000	Transition Count Ch 1	R
0x3080	Transition Count Ch 2	R
0x3100	Transition Count Ch 3	R
0x3180	Transition Count Ch 4	R
0x3200	Transition Count Ch 5	R
0x3280	Transition Count Ch 6	R
0x3300	Transition Count Ch 7	R
0x3380	Transition Count Ch 8	R
0x3400	Transition Count Ch 9	R
0x3480	Transition Count Ch 10	R
0x3500	Transition Count Ch 11	R
0x3580	Transition Count Ch 12	R

0x3600	Transition Count Ch 13	R
0x3680	Transition Count Ch 14	R
0x3700	Transition Count Ch 15	R
0x3780	Transition Count Ch 16	R
0x3800	Transition Count Ch 17	R
0x3880	Transition Count Ch 18	R
0x3900	Transition Count Ch 19	R
0x3980	Transition Count Ch 20	R
0x3A00	Transition Count Ch 21	R
0x3A80	Transition Count Ch 22	R
0x3B00	Transition Count Ch 23	R
0x3B80	Transition Count Ch 24	R

4.1.1.3 Frequency Measurement Registers

0x3014	***Frequency Measurement Period Ch 1***	R/W
0x3094	***Frequency Measurement Period Ch 2***	R/W
0x3114	***Frequency Measurement Period Ch 3***	R/W
0x3194	***Frequency Measurement Period Ch 4***	R/W
0x3214	***Frequency Measurement Period Ch 5***	R/W
0x3294	***Frequency Measurement Period Ch 6***	R/W
0x3314	***Frequency Measurement Period Ch 7***	R/W
0x3394	***Frequency Measurement Period Ch 8***	R/W
0x3414	***Frequency Measurement Period Ch 9***	R/W
0x3494	***Frequency Measurement Period Ch 10***	R/W
0x3514	***Frequency Measurement Period Ch 11***	R/W
0x3594	***Frequency Measurement Period Ch 12***	R/W

0x3614	***Frequency Measurement Period Ch 13***	R/W
0x3694	***Frequency Measurement Period Ch 14***	R/W
0x3714	***Frequency Measurement Period Ch 15***	R/W
0x3794	***Frequency Measurement Period Ch 16***	R/W
0x3814	***Frequency Measurement Period Ch 17***	R/W
0x3894	***Frequency Measurement Period Ch 18***	R/W
0x3914	***Frequency Measurement Period Ch 19***	R/W
0x3994	***Frequency Measurement Period Ch 20***	R/W
0x3A14	***Frequency Measurement Period Ch 21***	R/W
0x3A94	***Frequency Measurement Period Ch 22***	R/W
0x3B14	***Frequency Measurement Period Ch 23***	R/W
0x3B94	***Frequency Measurement Period Ch 24***	R/W

4.1.2 Output Mode Registers

4.1.2.1 PWM Registers

0x3014	***PWM Period Ch 1***	R/W
0x3094	***PWM Period Ch 2***	R/W
0x3114	***PWM Period Ch 3***	R/W
0x3194	***PWM Period Ch 4***	R/W
0x3214	***PWM Period Ch 5***	R/W
0x3294	***PWM Period Ch 6***	R/W
0x3314	***PWM Period Ch 7***	R/W
0x3394	***PWM Period Ch 8***	R/W
0x3414	***PWM Period Ch 9***	R/W
0x3494	***PWM Period Ch 10***	R/W
0x3514	***PWM Period Ch 11***	R/W
0x3594	***PWM Period Ch 12***	R/W

0x3614	***PWM Period Ch 13***	R/W
0x3694	***PWM Period Ch 14***	R/W
0x3714	***PWM Period Ch 15***	R/W
0x3794	***PWM Period Ch 16***	R/W
0x3814	***PWM Period Ch 17***	R/W
0x3894	***PWM Period Ch 18***	R/W
0x3914	***PWM Period Ch 19***	R/W
0x3994	***PWM Period Ch 20***	R/W
0x3A14	***PWM Period Ch 21***	R/W
0x3A94	***PWM Period Ch 22***	R/W
0x3B14	***PWM Period Ch 23***	R/W
0x3B94	***PWM Period Ch 24***	R/W

0x3010	***PWM Pulse Width Ch 1***	R/W
0x3090	***PWM Pulse Width Ch 2***	R/W
0x3110	***PWM Pulse Width Ch 3***	R/W
0x3190	***PWM Pulse Width Ch 4***	R/W
0x3210	***PWM Pulse Width Ch 5***	R/W
0x3290	***PWM Pulse Width Ch 6***	R/W
0x3310	***PWM Pulse Width Ch 7***	R/W
0x3390	***PWM Pulse Width Ch 8***	R/W
0x3410	***PWM Pulse Width Ch 9***	R/W
0x3490	***PWM Pulse Width Ch 10***	R/W
0x3510	***PWM Pulse Width Ch 11***	R/W
0x3590	***PWM Pulse Width Ch 12***	R/W
0x3018	***PWM Number of Cycles Ch 1***	R/W
0x3098	***PWM Number of Cycles Ch 2***	R/W

0x3610	***PWM Pulse Width Ch 13***	R/W
0x3690	***PWM Pulse Width Ch 14***	R/W
0x3710	***PWM Pulse Width Ch 15***	R/W
0x3790	***PWM Pulse Width Ch 16***	R/W
0x3810	***PWM Pulse Width Ch 17***	R/W
0x3890	***PWM Pulse Width Ch 18***	R/W
0x3910	***PWM Pulse Width Ch 19***	R/W
0x3990	***PWM Pulse Width Ch 20***	R/W
0x3A10	***PWM Pulse Width Ch 21***	R/W
0x3A90	***PWM Pulse Width Ch 22***	R/W
0x3B10	***PWM Pulse Width Ch 23***	R/W
0x3B90	***PWM Pulse Width Ch 24***	R/W
0x3618	***PWM Number of Cycles Ch 13***	R/W
0x3698	***PWM Number of Cycles Ch 14***	R/W

0x3118	***PWM Number of Cycles Ch 3***	R/W
0x3198	***PWM Number of Cycles Ch 4***	R/W
0x3218	***PWM Number of Cycles Ch 5***	R/W
0x3298	***PWM Number of Cycles Ch 6***	R/W
0x3318	***PWM Number of Cycles Ch 7***	R/W
0x3398	***PWM Number of Cycles Ch 8***	R/W
0x3418	***PWM Number of Cycles Ch 9***	R/W
0x3498	***PWM Number of Cycles Ch 10***	R/W
0x3518	***PWM Number of Cycles Ch 11***	R/W
0x3598	***PWM Number of Cycles Ch 12***	R/W

0x3718	***PWM Number of Cycles Ch 15***	R/W
0x3798	***PWM Number of Cycles Ch 16***	R/W
0x3818	***PWM Number of Cycles Ch 17***	R/W
0x3898	***PWM Number of Cycles Ch 18***	R/W
0x3918	***PWM Number of Cycles Ch 19***	R/W
0x3998	***PWM Number of Cycles Ch 20***	R/W
0x3A18	***PWM Number of Cycles Ch 21***	R/W
0x3A98	***PWM Number of Cycles Ch 22***	R/W
0x3B18	***PWM Number of Cycles Ch 23***	R/W
0x3B98	***PWM Number of Cycles Ch 24***	R/W

0x200C	***PWM Output Polarity***	R/W

4.1.2.2 Pattern Generator Registers

0x0004 0000 to 0x0007 FFFC	***Pattern RAM***	R/W

0x2010	***Pattern RAM Period***	R/W
0x2014	***Pattern RAM Start Address***	R/W
0x2018	***Pattern RAM End Address***	R/W
0x201C	***Pattern RAM Control***	R/W
0x2020	***Pattern RAM Number of Cycles***	R/W

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Status and Interrupts

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	6/17/2019	Initial release	GC
A1	4/22/2020	ECO C07519: Module manuals updated for formatting consistency. No technical or specification updates.	MC

Table of Contents

1 Status and Interrupts

Status registers indicate the detection of faults or events. The status registers can be channel bit-mapped or event bit-mapped. An example of a channel bit-mapped register is the BIT status register, and an example of an event bit-mapped register is the FIFO status register.

For those status registers that allow interrupts to be generated upon the detection of the fault or the event, there are four registers associated with each status: *Dynamic, Latched, Interrupt Enabled*, and *Set Edge/Level Interrupt*.

Dynamic Status: The *Dynamic Status* register indicates the *current* condition of the fault or the event. If the fault or the event is momentary, the contents in this register will be clear when the fault or the event goes away. The *Dynamic Status* register can be polled, however, if the fault or the event is sporadic, it is possible for the indication of the fault or the event to be missed.

Latched Status: The *Latched Status* register indicates whether the fault or the event *has occurred* and keeps the state until it is cleared by the user. Reading the *Latched Status* register is a better alternative to polling the *Dynamic Status* register because the contents of this register will not clear until the user commands to clear the specific bit(s) associated with the fault or the event in the *Latched Status* register. Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel/event) location will "clear" the bit (set the bit to **0**). When clearing the channel/event bits, it is strongly recommended to write back the same bit pattern as read from the *Latched Status* register. For example, if the channel bit-mapped *Latched Status* register contains the value 0x0000 0005, which indicates fault/event detection on channel 1 and 3, write the value 0x0000 0005 to the *Latched Status* register to clear the fault/event status for channel 1 and 3. Writing a "1" to other channels that are not set (example 0x0000 000F) may result in incorrectly "clearing" incoming faults/events for those channels (example, channel 2 and 4).

Interrupt Enable: If interrupts are preferred upon the detection of a fault or an event, enable the specific channel/event interrupt in the *Interrupt Enable* register. The bits in *Interrupt Enable* register map to the same bits in the *Latched Status* register. When a fault or event occurs, an interrupt will be fired. Subsequent interrupts will not trigger until the application acknowledges the fired interrupt by clearing the associated channel/event bit in the *Latched Status* register. If the interruptible condition is still persistent after clearing the bit, this may retrigger the interrupt depending on the *Edge/Level* setting.

Set Edge/Level Interrupt: When interrupts are enabled, the condition on retriggering the interrupt after the Latch Register is "cleared" can be specified as "edge" triggered or "level" triggered. Note, the Edge/Level Trigger also affects how the Latched Register value is adjusted after it is "cleared" (see 1.1.1).

- *Edge triggered*: An interrupt will be retriggered when the Latched Status register change from low (0) to high (1) state. Uses for edge-triggered interrupts would include transition detections (Low-to-High transitions, High-to-Low transitions) or fault detections. After "clearing" an interrupt, another interrupt will not occur until the next transition or the re-occurrence of the fault again.
- *Level triggered*: An interrupt will be generated when the Latched Status register remains at the high (1) state. Level-triggered interrupts are used to indicate that something needs attention.

1.1 Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed with a unique number/identifier defined by the user such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism. In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

1.2 Interrupt Trigger Types

In most applications, limiting the number of interrupts generated is preferred as interrupts are costly, thus choosing the correct Edge/Level interrupt trigger to use is important.

Example 1: Fault detection

This example illustrates interrupt considerations when detecting a fault like an “open” on a line. When an “open” is detected, the system will receive an interrupt. If the “open” on the line is persistent and the trigger is set to “edge”, upon “clearing” the interrupt, the system will not re-generate another interrupt. If, instead, the trigger is set to “level”, upon “clearing” the interrupt, the system will re-generate another interrupt. Thus, in this case, it will be better to set the trigger type to “edge”.

Example 2: Threshold detection

This example illustrates interrupt considerations when detecting an event like reaching or exceeding the “high watermark” threshold value. In a communication device, when the number of elements received in the FIFO reaches the high-watermark threshold, an interrupt will be generated. Normally, the application would read the count of the number of elements in the FIFO and read this number of elements from the FIFO. After reading the FIFO data, the application would “clear” the interrupt. If the trigger type is set to “edge”, another interrupt will be generated only if the number of elements in FIFO goes below the “high watermark” after the “clearing” the interrupt and then fills up to reach the “high watermark” threshold value. Since receiving communication data is inherently asynchronous, it is possible that data can continue to fill the FIFO as the application is pulling data off the FIFO. If, at the time the interrupt is “cleared”, the number of elements in the FIFO is at or above the “high watermark”, no interrupts will be generated. In this case, it will be better to set the trigger type to “level”, as the purpose here is to make sure that the FIFO is serviced when the number of elements exceeds the high watermark threshold value. Thus, upon “clearing” the interrupt, if the number of elements in the FIFO is at or above the “high watermark” threshold value, another interrupt will be generated indicating that the FIFO needs to be serviced.

1.3 Dynamic and Latched Status Registers Examples

The examples in this section illustrate the differences in behavior of the Dynamic Status and Latched Status registers as well as the differences in behavior of Edge/Level Trigger when the Latched Status register is cleared.

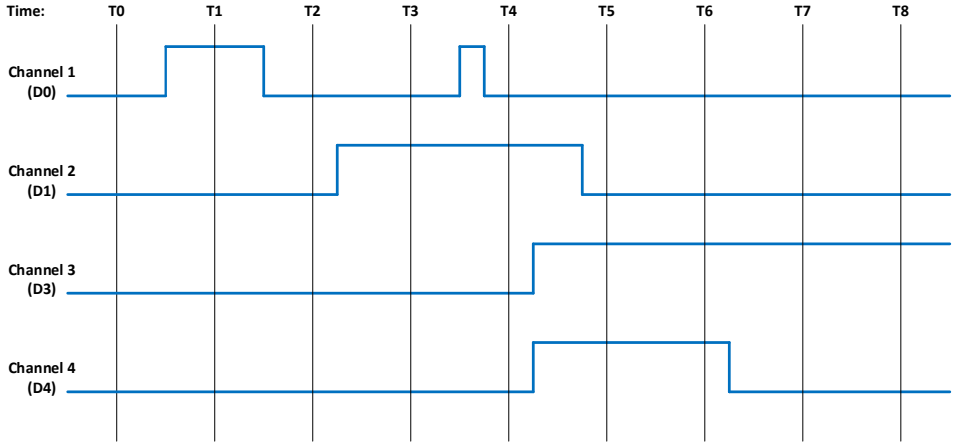

Figure 1 - Example of Module's Channel-Mapped Dynamic and Latched Status States

Time	Dynamic Status	No Clearing of Latched Status	Clearing of Latched Status (Edge-Triggered)		Clearing of Latched Status (Level-Triggered)	
		Latched Status	Action	Latched Status	Action	Latched
T0	0x0	0x0	Read Latched Register	0x0	Read Latched Register	0x0
T1	0x1	0x1	Read Latched Register	0x1		0x1
			Write 0x1 to Latched Register		Write 0x1 to Latched Register	
				0x0		*0x1*
T2	0x0	0x1	Read Latched Register	0x0	Read Latched Register	0x1
					Write 0x1 to Latched Register	
						0x0
T3	0x2	0x3	Read Latched Register	0x2	Read Latched Register	0x2
			Write 0x2 to Latched Register		Write 0x2 to Latched Register	
				0x0		*0x2*
T4	0x2	0x3	Read Latched Register	0x1	Read Latched Register	0x3
			Write 0x1 to Latched Register		Write 0x3 to Latched Register	
				0x0		*0x2*
T5	0xC	0xF	Read Latched Register	0xC	Read Latched Register	0xE
			Write 0xC to Latched Register		Write 0xE to Latched Register	
				0x0		*0xC*
T6	0xC	0xF	Read Latched Register	0x0	Read Latched Register	0xC
					Write 0xC to Latched Register	
						0xC
T7	0x4	0xF	Read Latched Register	0x0	Read Latched Register	0xC
					Write 0xC to Latched Register	
						0x4
T8	0x4	0xF	Read Latched Register	0x0	Read Latched Register	0x4

1.4 Interrupt Examples

The examples in this section illustrate the interrupt behavior with Edge/Level Trigger.

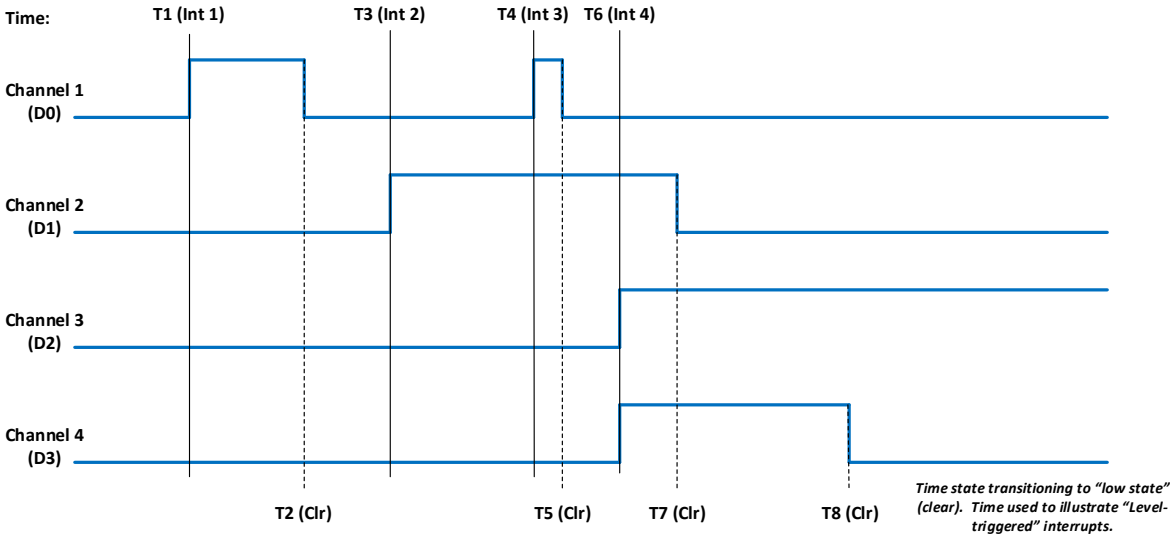

Figure 2 - Illustration of Latched Status State for Module with 4-Channels with Interrupt Enabled

Time	Latched Status (Edge-Triggered – Clear Multi-Channel) Action	Latched	Latched Status (Edge-Triggered – Clear Single Channel) Action	Latched	Latched Status (Level-Triggered – Clear Multi-Channel) Action	Latched
T1 (Int 1)	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1
	Write 0x1 to Latched Register		Write 0x1 to Latched Register		Write 0x1 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T2.	*0x1*
T3 (Int 2)	**Interrupt Generated** Read Latched Registers	0x2	**Interrupt Generated** Read Latched Registers	0x2	**Interrupt Generated** Read Latched Registers	0x2
	Write 0x2 to Latched Register		Write 0x2 to Latched Register		Write 0x2 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T7.	*0x2*
T4 (Int 3)	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x3
	Write 0x1 to Latched Register		Write 0x1 to Latched Register		Write 0x3 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0x3 is reported in Latched Register until T5.	*0x3*
					Interrupt re-triggers Note, interrupt re-triggers after each clear until T7.	*0x2*

T6 (Int 4)	**Interrupt Generated** Read Latched Registers	0xC	**Interrupt Generated** Read Latched Registers	0xC	**Interrupt Generated** Read Latched Registers	0xE
	Write 0xC to Latched Register		Write 0x4 to Latched Register		Write 0xE to Latched Register	
		0x0	***Interrupt re-triggers*** Write 0x8 to Latched Register	*0x8*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xE is reported in Latched Register until T7.	*0xE*
				0x0	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xC is reported in Latched Register until T8.	*0xC*
					Interrupt re-triggers Note, interrupt re-triggers after each clear and 0x4 is reported in Latched Register always.	*0x4*

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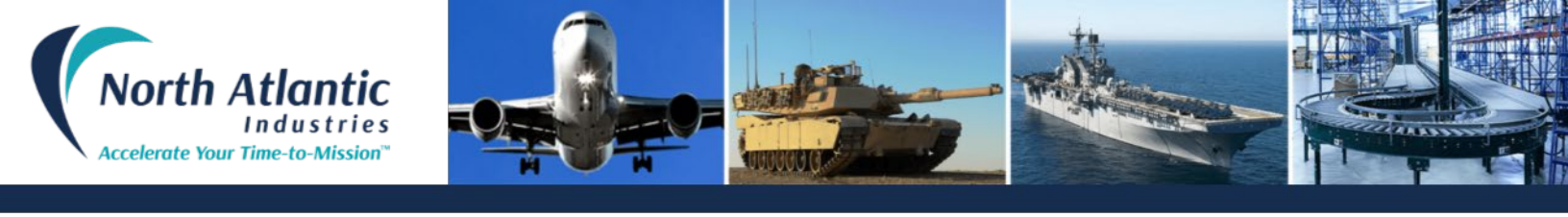

User Watchdog Timer

MODULE MANUAL
APPENDIX

Revision History

Revision	Revision Date	Description	Draft/Apprv.
A	6/25/2019	Initial release	GC
A1	10/7/2019	Appended “User” to Watchdog Timer to indicate that the Watchdog Timer is controlled by the user’s application.	GC
A2	4/22/2020	ECO C07519: Module manuals updated for formatting consistency. No technical or specification updates.	MC
B	3/29/2021	ECO C08381: Re-identified Digital-to-Synchro/Resolver (D/S) or Digital-to-L(R)VDT (D/LV) Modules are currently unsupported (at this time).	ARS

Table of Contents

1 User Watchdog Timer Module Manual

1.1 User Watchdog Timer Capability

The User Watchdog Timer (UWDT) Capability is available on the following modules:

- AC Reference Source Modules
  - AC1 – 1 Channel, 2-115 Vrms, 47 Hz – 20kHz
  - AC2 – 2 Channels, 2-28 Vrms, 47 Hz – 20kHz
  - AC3 – 1 Channel, 28-115 Vrms, 47 Hz – 2.5 kHz
- Differential Transceiver Modules
  - DF1/DF2 – 16 Channels Differential I/O
- Digital-to-Analog (D/A) Modules
  - DA1 – 12 Channels, ±10 VDC @ 25 mA, Voltage or Current Control Modes
  - DA2 – 16 Channels, ±10 VDC @ 10 mA
  - DA3 – 4 Channels, ±40 VDC @ ±100 mA, Voltage or Current Control Modes
  - DA4 – 4 Channels, ±80 VDC @ 10 mA
  - DA5 - 4 Channels, ±65 VDC or ±2 A, Voltage or Current Control Modes
- Digital-to-Synchro/Resolver (D/S) or Digital-to-L(R)VDT (D/LV) Modules

  (Not supported)
- Discrete I/O Modules
  - DT1/DT4 – 24 Channels, Programmable for either input or output, output up to 500 mA per channel from an applied external 3 – 60 VCC source.
  - DT2/DT5 – 16 Channels, Programmable for either input voltage measurements (±80 V) or as a bi-directional current switch (up to 500 mA per channel).
  - DT3/DT6 – 4 Channels, Programmable for either input voltage measurements (±100 V) or as a bi-directional current switch (up to 3 A per channel).
- TTL/CMOS Modules
  - TL1-TL8 – 24 Channels, Programmable for either input or output.

1.2 Principle of Operation

The User Watchdog Timer is optionally activated by the applications that require the module's outputs to be disabled as a failsafe in the event of an application failure or crash. The circuit is designed such that a specific periodic write strobe pattern must be executed by the software to maintain operation and prevent the disablement from taking place.

The User Watchdog Timer is inactive until the application sends an initial strobe by writing the value 0x55AA to the *UWDT Strobe* register. After activating the User Watchdog Timer, the application must continually strobe the timer within the intervals specified with the configurable *UWDT Quiet Time* and *UWDT Window* registers. The timing of the strobes must be consistent with the following rules:

- The application must not strobe during the Quiet time.
- The application must strobe within the Window time.
- The application must not strobe more than once in a single window time.

A violation of any of these rules will trigger a User Watchdog Timer fault and result in shutting down any isolated power supplies and/or disabling any active drive outputs, as applicable for the specific module. Upon a User Watchdog Timer event, recovery to the module shutting down will require the module to be reset.

The Figure 1 and Figure 2 provides an overview and an example with actual values for the User Watchdog Timer Strobes, Quiet Time and Window. As depicted in the diagrams, there are two processes that run in parallel. The Strobe event starts the timer for the beginning of the "Quiet Time". The timer for the Previous Strobe event continues to run to ensure that no additional Strobes are received within the "Window" associated with the Previous Strobe.

The optimal target for the user watchdog strobes should be at the interval of [Quiet time + ½ Window time] after the previous strobe, which will place the strobe in the center of the window. This affords the greatest margin of safety against unintended disablement in critical operations.

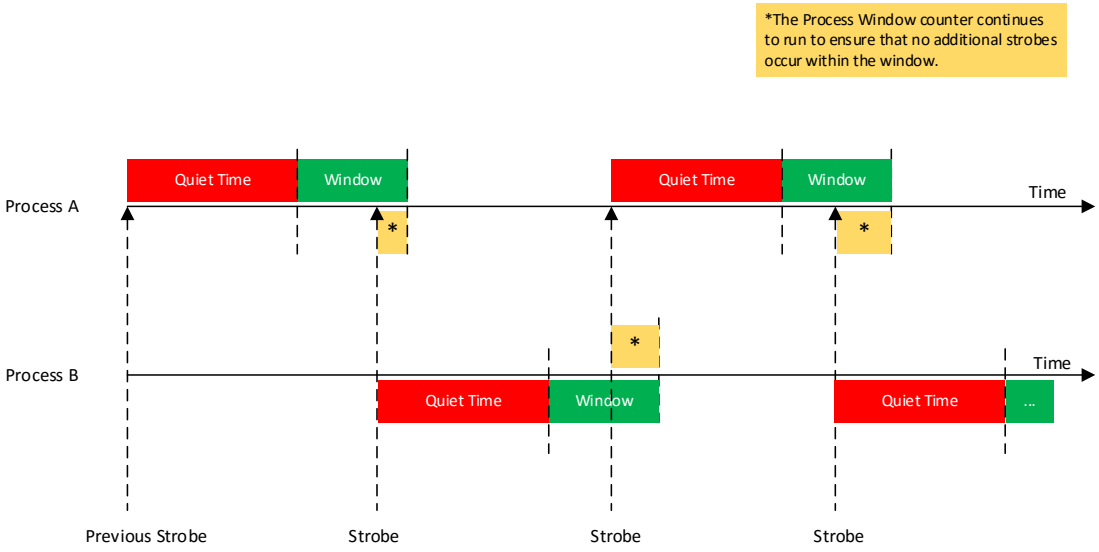

Figure 1 – User Watchdog Timer Overview

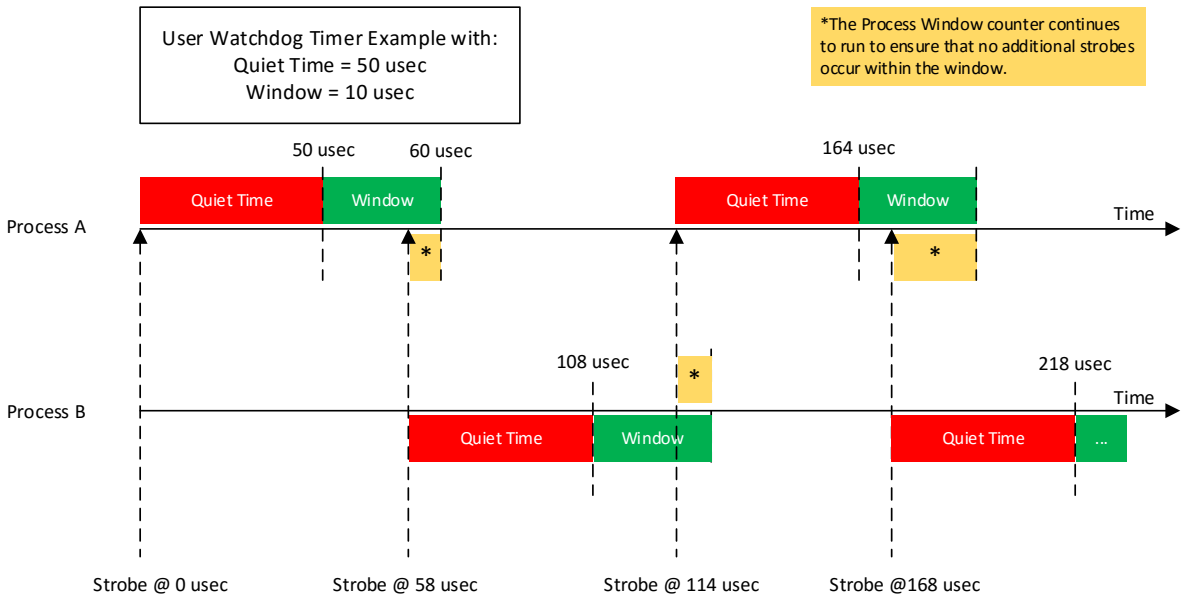

Figure 2 – User Watchdog Timer Example

Figure 3 illustrates examples of User Watchdog Timer failures.

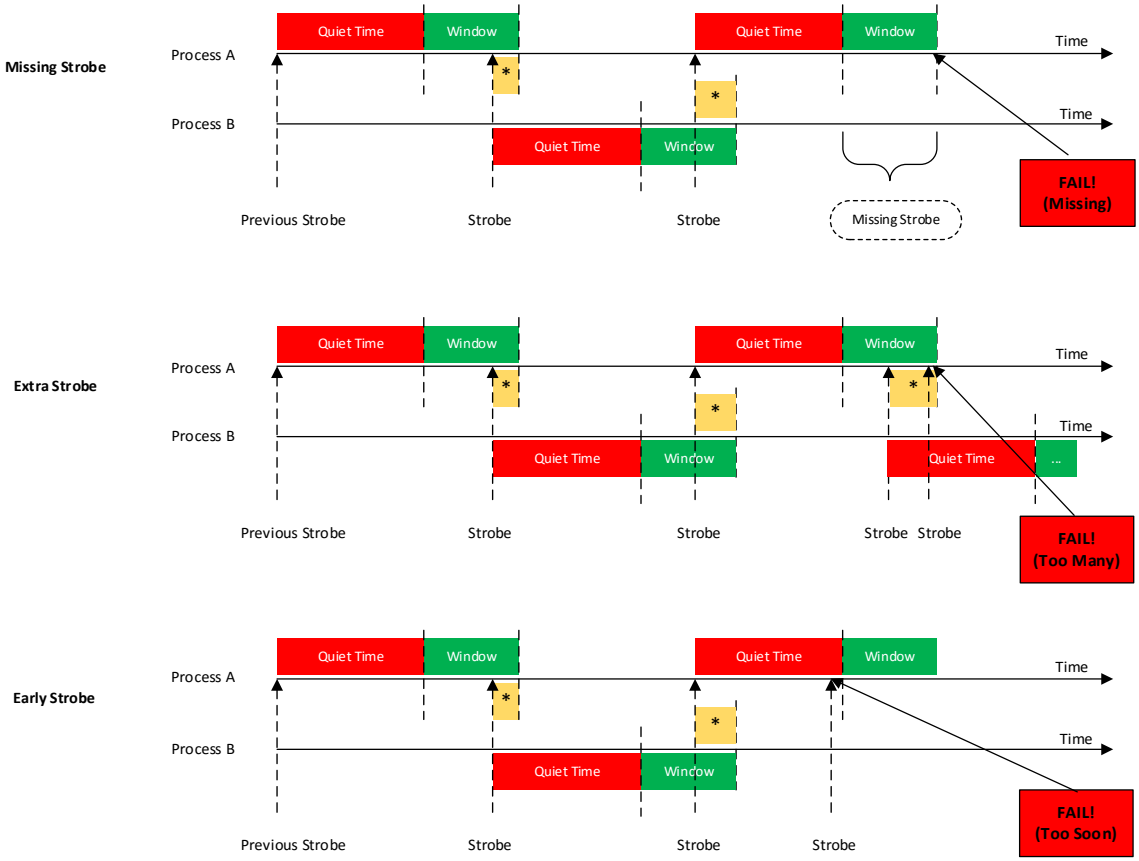

Figure 3 – User Watchdog Timer Failures

1.3 Register Descriptions

The register descriptions provide the register name, Type, Data Range, Read or Write information, Initialized Value, and a description of the function.

1.3.1 User Watchdog Timer Registers

The registers associated with the User Watchdog Timer provide the ability to specify the *UWDT Quiet Time* and the *UWDT Window* that will be monitored to ensure that EXACTLY ONE User Watchdog Timer (UWDT) Strobe is written within the window.

1.3.1.1 UWDT Quiet Time

Function: Sets Quiet Time value (in microseconds) to use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0 µsec to 2^32 µsec (0x0 to 0xFFFFFFFF)

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: LSB = 1 µsec. The application must NOT write a strobe in the time between the previous strobe and the end of the Quiet time interval. In addition, the application must write in the *UWDT Window* EXACTLY ONCE.

1.3.1.2 UWDT Window

Function: Sets Window value (in microseconds) to use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0 µsec to 2^32 µsec (0x0 to 0xFFFFFFFF)

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: LSB = 1 µsec. The application must write the strobe once within the Window time after the end of the Quiet time interval. The application must write in the *UWDT Window* EXACTLY ONCE.

This setting must be initialized to a non-zero value for operation and should allow sufficient tolerance for strobe timing by the application.

1.3.1.3 UWDT Strobe

Function: Writes the strobe value to be use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0x55AA

Read/Write: W

Initialized Value: 0x0

Operational Settings: At startup, the user watchdog is disabled. Write the value of 0x55AA to this register to start the user watchdog timer monitoring after initial power on or a reset. To prevent a disablement, the application must periodically write the strobe based on the user watchdog timer rules.

1.3.2 Status and Interrupt

The modules that are capable of User Watchdog Timer support provide status registers for the User Watchdog Timer.

1.3.2.1 User Watchdog Timer Status

The status register that contains the User Watchdog Timer Fault information is also used to indicate channel Inter-FPGA failures on modules that have communication between FPGA components. There are four registers associated with the User Watchdog Timer Fault/Inter-FPGA Failure Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt*.

User Watchdog Timer Fault/Inter-FPGA Failure Dynamic Status		
User Watchdog Timer Fault/Inter-FPGA Failure Latched Status		
User Watchdog Timer Fault/Inter-FPGA Failure Interrupt Enable		
User Watchdog Timer Fault/Inter-FPGA Failure Set Edge/Level Interrupt		
Bit(s)	**Status**	**Description**
D31	User Watchdog Timer Fault Status	**0** = No Fault **1** = User Watchdog Timer Fault
D30:D0	Reserved for Inter-FPGA Failure Status	Channel bit-mapped indicating channel inter-FPGA communication failure detection.

Function: Sets the corresponding bit (D31) associated with the channel's User Watchdog Timer Fault error.
Type: unsigned binary word (32-bit)
Data Range: 0x0000 0000 to 0xFFFF FFFF
Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)
Initialized Value: 0

1.3.2.2 Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed (typically with a unique number/identifier) such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism.

In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

Note, the Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Common Memory and these registers are associated with the Module Slot position (refer to Function Register Map).

1.3.2.3 Interrupt Vector

Function: Set an identifier for the interrupt.
Type: unsigned binary word (32-bit)
Data Range: 0x0000 0000 to 0xFFFF FFFF
Read/Write: R/W
Initialized Value: 0
Operational Settings: When an interrupt occurs, this value is reported as part of the interrupt mechanism.

1.3.2.4 Interrupt Steering

Function: Sets where to direct the interrupt.
Type: unsigned binary word (32-bit)
Data Range: See table
Read/Write: R/W
Initialized Value: 0
Operational Settings: When an interrupt occurs, the interrupt is sent as specified:

Direct Interrupt to VME	1
Direct Interrupt to ARM Processor (via SerDes) *(Custom App on ARM or NAI Ethernet Listener App)*	2
Direct Interrupt to PCIe Bus	5
Direct Interrupt to cPCI Bus	6

1.3.3 Function Register Map

Key: ***Bold Italic = Configuration/Control***

Bold Underline = Status

*When an event is detected, the bit associated with the event is set in this register and will remain set until the user clears the event bit. Clearing the bit requires writing a 1 back to the specific bit that was set when read (i.e. write-1-to-clear, writing a '1' to a bit set to '1' will set the bit to '0').

1.3.3.1 User Watchdog Timer Registers

0x01C0	***UWDT Quiet Time***	R/W
0x01C4	***UWDT Window***	R/W
0x01C8	***UWDT Strobe***	W

1.3.3.2 Status Registers

User Watchdog Timer Fault/Inter-FPGA Failure

0x09B0	**Dynamic Status**	R
0x09B4	**Latched Status***	R/W
0x09B8	***Interrupt Enable***	R/W
0x09BC	***Set Edge/Level Interrupt***	R/W

1.3.3.3 Interrupt Register

The Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Memory Space and these addresses are absolute based on the module slot position. In other words, do not apply the Module Address offset to these addresses.

0x056C	***Module 1 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x066C	***Module 1 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x076C	***Module 2 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x086C	***Module 2 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x096C	***Module 3 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0A6C	***Module 3 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0B6C	***Module 4 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0C6C	***Module 4 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0D6C	***Module 5 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0E6C	***Module 5 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0F6C	***Module 6 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x106C	***Module 6 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W

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